Optimal Control of Multilevel Flying-Capacitor Converters

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The candidate confirms that the work submitted is his own and that appropriate credit has been given where reference has been made to the work of others.

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Abstract

This thesis is concerned with the flying-capacitor multilevel power converter topology. This converter is one of several different static power converter circuits which can produce three or more distinct voltage levels at the output terminals. All multilevel converters are constructed from semiconductor power switches which have a lower voltage rating than the maximum terminal voltages, and so are generally used in high power, medium voltage applications. Flying-capacitor converters have internal floating capacitors which provide voltage clamping of the power switches. To ensure correct operation, the internal capacitor voltages have to be at specific balanced levels and this poses a major challenge in the control of the flying-capacitor converter.

The main objective of this work was to investigate the control of a three-phase flying-capacitor inverter, and identify optimal modulation strategies which would improve the output power quality by minimising the harmonic content of the output waveforms. As part of this investigation, suitable capacitor voltage balancing strategies for incorporation within the modulation control system had to be identified. It was also the intention of the work to quantify the effect on performance of different capacitor ratings, in order to provide a definitive guide to selecting components for a practical inverter.

Simulations of various forms of multilevel sinusoidal modulation are presented in the thesis. The modulation schemes covered are selective harmonic elimination (SHE), sine-triangle PWM and space vector PWM. In the flying-capacitor inverter, there are a variety of different implementations possible for each scheme due to the increased number of synthesisable output voltage levels. The relative merits of the different modulators are assessed based on output power quality, and this is done in respect to the novel capacitor voltage balancing strategies developed for each scheme. To aid this investigation, a detailed simulator program has been developed which incorporates realistic models of the inverter system and digital controller.

The investigations into SHE control have revealed that a switching state rotation pattern can be optimally selected to balance the capacitor voltages and actually reduce the harmonic content of the output in the case of practically sized capacitors. System characteristics are presented which can enable the selection of the capacitors based on the load characteristic in order to optimise the performance of the practical inverter.

An in-depth investigation into the various sine-triangle PWM carrier placement options, reference sampling methods and hardware implementation issues known in the literature has been carried out. The results show the effect of the various implementations on output power quality and a comparative assessment is presented in the context of practical sized capacitors. A novel digital hardware-based capacitor

voltage balancing control scheme is proposed and shown to work well without the need of voltage sensors on the capacitors.

Space vector PWM is investigated and a very simple approach to computation of the duty cycles using a carrier-based implementation to generate the space vector firing pattern is presented. It is shown to give the same results as more complex algorithms adopted in the past, aimed at the selection of the synthesising vectors from the large number of switching state vectors in the multilevel inverter. The novel PWM balancing strategy ensures that the inverter operates correctly in a balanced state.

An experimental three-phase, five-level inverter has been constructed and used to confirm the validity of the simulation work. Results presented show that the inverter operates correctly, with balanced capacitor voltages, under all forms of sinusoidal modulation control.

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List of Principle Symbols

Symbol	**Meaning**	**Units**
N	number of inverter cells	
V_{dc}	dc link voltage	Volt
V_{level}	inverter level voltage	Volt
V_1	fundamental voltage	Volt
f_1	fundamental frequency	Hertz
ω_1	angular fundamental frequency	radian/s
ϕ	angular displacement between voltage and current fundamentals	radian
$\cos\phi$	displacement power factor	
α	control firing angle	radian
m_a	amplitude modulation index	
m_f	frequency modulation index	
D	PWM duty cycle	
T_s	PWM switching period	second
$\mathbf{V}$	voltage space vector	Volt
m	voltage level	
LEV	number of states	
SEQ	number of switching sequences	
P	number of patterns	
B	number of balancing cycles	
$\mathbf{V_C}$	cell-capacitor voltage vector	Volt
$\mathbf{J}$	Jordan switching state control matrix	
$\mathbf{S}$	switching state vector	
$\mathbf{C}$	capacitor matrix	$Farad^{-1}$
E_c	energy stored in a unit cell-capacitor	Joule
ξ	energy factor	s^{-1}

All others symbols have their usually accepted meaning.

List of Abbreviations

AFE	active front-end
APOD	alternative phase opposition disposition
ASIC	application specific integrated circuit
CAD	computer-aided design
CLK	clock
CSI	current source inverter
DF1	distortion factor 1
DF2	distortion factor 2
DPF	displacement power factor
DPS	disposed phase shift
DSP	digital signal processor
EMC	electromagnetic compatibility
FACTS	flexible alternating current transmission system
FFT	fast Fourier transform
FPGA	field programmable gate array
GTO	gate-turn-off thyristor
GUI	graphical user interface
HPS	hybrid phase shift
HVDC	high-voltage direct current
IGBT	insulated gate bipolar transistor
IGCT	insulated gate-commutated thyristor
SCR	silicon controlled rectifier
MOSFET	metal oxide semiconductor field effect transistor
MUX	multiplexer
NPC	neutral point clamped
OOP	object oriented programming
PCB	printed circuit board
PD	phase disposition
PF	power factor
PFC	power factor correction
PI	proportional integral
PIN	positive-intrinsic-negative
PLL	phase locked loop
POD	phase opposition disposition
PS	phase shift
PWM	pulse width modulation
RFI	radio frequency interference

ROM	read-only memory
STATCOM	static compensator
SHE	selective harmonic elimination
SHE-4H2	SHE four cell two harmonics
SHE-4H4	SHE four cell four harmonics
SMPS	switched-mode power supply
SPD	shifted phase disposition
SPOD	shifted phase opposition disposition
SPWM	sinusoidal pulse width modulation
SVPWM	space vector pulse width modulation
THD	total harmonic distortion
TPF	true power factor
UPFC	unified power flow controller
UPLC	universal power line conditioner
UPS	uninterruptible power system
VAr	volt-ampere reactive
VCOX	voltage controlled oscillator crystal
VHDL	VHSIC hardware description language
VHSIC	very high speed integrated circuit
VSI	voltage source inverter
WTHD	weighted total harmonic distortion
ZCT	zero current transition
ZVT	zero voltage transition