Chapter 7 CONCLUSIONS

7.1 Achievements

This thesis has reported a comprehensive investigation into the various forms of modulation control applicable to the flying-capacitor multilevel converter, specifically in relation to the synthesis of sinusoidal output voltages with low harmonic distortion when the topology is employed as an inverter. In this context, the issues of system balancing and the effect of the circuit parameters on performance have been addressed. The major achievements and contributions of this work are summarised as follows:

- A detailed understanding of the cell-capacitor voltage balancing requirements has been demonstrated. It has been shown by using basic circuit analysis that a self-balancing mechanism is inherent to the topology when the averaged duty cycles of each cell switch pair are the same for a given output voltage level.
- A comprehensive simulator program has been developed which includes accurate models of the different components and of the digital control implementation. This has allowed a thorough investigation of sinusoidal modulation and aided the design of an experimental inverter.
- Selective harmonic elimination control has been investigated, specifically in the staircase voltage case. A switching pattern balancing scheme has been developed which ensures that the mean cell-capacitor voltages are at the correct operating levels. The scheme works well in the steady-state and it has been shown that load transient events do not upset the balancing.
- The issue of sub- and inter-harmonic generation has been addressed for the first time in a flying-capacitor inverter with practical sized cell-capacitors. It has been shown that there is a relationship between the capacitor ripple voltage and cycle by cycle balancing strategy and harmonic distortion. It has also been demonstrated that selecting the optimal balancing pattern can improve performance by reducing the harmonics.
- The relationship between the stored energy in the cell-capacitors and the load characteristic has been investigated and a set of normalised curves produced which identify the effect of the cell-capacitance on maximum semiconductor switch blocking voltage and output voltage THD under staircase control.

- The different forms of sine-triangle PWM implementation have been investigated and their relative merits assessed. Practical implementation issues such as reference sampling, digital logic clock frequency and dead-time have all been covered in the analysis.
- A novel balancing scheme has been developed based on a sub-carrier gate-firing rotation which is applicable to all forms of fixed frequency PWM, and which is simple to implement in digital hardware. It has been shown that the digital logic timings are critical for balanced operation and a novel method for ensuring that the timing errors are minimised has been proposed.
- The normalised inverter system operating characteristics have been mapped as functions of the energy stored per unit cell capacitor and the load power factor. It is has been shown that the characteristic energy factor curve has the same form as SHE control and the relationship between switching frequency and maximum safe-operating output power quantified.
- Space vector PWM has been investigated in the context of a multilevel inverter and a simple algorithm has been developed to minimise the computational requirements. It has been shown that the output voltage harmonic distortion level is on a par with the third harmonic injected sine-triangle PWM scheme, and that these two modulation methods are in essence the same.
- An experimental four-cell, three-phase inverter has been constructed and the measured harmonic performance has been assessed. All forms of modulation control have been implemented and there is excellent correlation between the measured system operating parameters and the simulated performance.

7.2 Recommendations for Future Work

There are areas where the practical design of the flying-capacitor inverter can be improved. Firstly, the VCOX approach to optimising the timing of the digital control implementation needs to be validated in practice. Secondly, reductions in the timing delays associated with the interface circuitry between the digital controller and the gate-drivers are required to improve performance especially at higher switching frequency. Finally, it is envisaged that an improved gate drive circuit can be developed which includes a drain-source voltage monitor for detecting over-voltage conditions, and which can be part of a sensed cell-capacitor voltage balancing system.

Although the work presented has addressed all forms of sinusoidal voltage synthesis, and demonstrated practical implementations, there remains one area where a more

thorough understanding is required. The large number of switching states and the necessity for rotating these switching states to achieve cell-capacitor voltage balancing has the potential to introduce unstable or chaotic behaviour. This is an important area of interest especially concerning inverter operation with a stable closed-loop voltage controller.

The flying-capacitor multilevel inverter system can be used in a variety of different high power applications which are only recently becoming practical with modern electronic components. Motor drives are an important application for the inverter, and one specific area where a contribution could be made is in the effect on machine operating performance of harmonics present in the output voltage when operating under staircase control with the pattern-based balancing strategy employed.

Another possible area of research, where a significant contribution can be made, is in the use of the asymmetric bridge form of the flying-capacitor multilevel topology as the power converter stage in a switched reluctance motor drive. The availability of more than one voltage level has the potential to improve the operating performance of these machines over a much wider speed range than is possible using existing two-level power converters. Torque ripple could be reduced by exploiting the extra voltage control modes in profiling the chopped phase current at reduced switching frequency and therefore higher efficiency. Alternatively, the higher efficiency single-pulse voltage control mode can be extended down to lower speeds by reducing the phase operating voltage. The two most likely applications to benefit from this approach are traction where smoother torque is preferred and renewable energy systems, such as wind turbines, where generation would be possible at lower wind speeds than at present. This has the potential for reducing the size of the gearbox or even eliminating it.

The most exciting possibilities for future research on flying-capacitor inverter applications are in the area of power conditioning systems, such as reactive power controllers, active harmonic filters and unified power flow controllers. The necessity for a large number of capacitors in this type of multilevel inverter may well be less of an impediment, especially if the system control is optimised to make use of the available the stored energy. There is also potential in adjusting the internal cell-capacitor voltage variations in a favourable manner in terms of the resultant harmonic generation for cancelling unwanted harmonics in the utility supply system.

The simulator developed for analysing the performance of the flying-capacitor inverter and investigating the influence of the control strategy on performance is a useful tool which can aid further research on the inverter. The experimental inverter also provides an excellent laboratory facility for investigating further the practical performance of systems based on the flying-capacitor inverter.

Finally, some elements of this work have already been disseminated to the international community through the publication of six papers at various conferences. The paper bibliographies are listed in Appendix B. It is expected that an additional two journal papers will be published on the material contained in this thesis, and further conference papers may follow.