Chapter 5 SPACE VECTOR PWM

5.1 Introduction

The space vector PWM (SVPWM) [5.1] is an alternative method used to control three-phase inverters, where the PWM duty cycles are computed rather than derived through hardware comparison like sine-triangle PWM reviewed in detail in Chapter 4. In SVPWM, the three-phase stationary reference frame voltages for each inverter switching state are mapped to the complex two-phase orthogonal α-β plane. The reference voltage is represented as a vector in this plane and duty-cycles are computed for the selected switching state vectors in proximity to the reference. In multilevel inverters, the number of switching state vectors increases and this additional complexity has prompted many attempts at optimizing the performance of the SVPWM method for multilevel inverters.

This chapter focuses specifically on one simple multilevel SVPWM scheme which is relatively easy to implement in hardware. The aim is do a direct comparison with the other forms of control when applied to the flying-capacitor inverter.

5.2 Space-Vector Representation

Space vector modulation was developed from the concept that a set of three-phase waveforms can be represented by a single rotating vector. One of the earliest proposed modulation strategies to use this concept was by Murai et al. [5.2]. Space vector PWM developed fully in the late 1980s through the work of various researchers, notably Van der Broeck [5.3]. It was also applied to three-level inverters at that time through the work of Steinke [5.4] and Bauer and Heining [5.5].

The application of SVPWM to multilevel inverters developed throughout the 1990s with various schemes proposed in the literature. The larger number of switching states in a multilevel inverter proved challenging in developing optimum algorithms for the computation of duty cycles and selection of switching states at the different voltage levels. Lee et al. from Hanyang University [5.6] proposed a method of duty cycle computation which was based on the individual triangular regions between the multilevel switching states. A similar approach is been adopted for a generalised SVPWM algorithm developed by Wei, et al. from Ryerson University [5.7] which is aimed at the control of cascaded-cell multilevel inverters. An alternative computation

algorithm for computing the duty cycles has been proposed by Peng et al. from Virginia Polytechnic and State University [5.8].

Zhang et al. from Oregon State University [5.9] investigated switching state selection in order to eliminate common-mode voltages. Li et al. from two New York State universities [5.10] developed a multilevel SVPWM scheme by creating two phase shifted vectors to represent the actual reference vector. They developed this algorithm specifically for the cascaded-cell multilevel inverter where the requirements for cell-capacitor voltage balancing are not present. Also of interest is the work of Filho et al. [5.11], who have applied artificial neural networks (ANN) to the problem of sector identification and duty cycle computation.

It has been appreciated since the beginning of SVPWM development that there is a correlation between the carrier-based PWM scheme and SVPWM [5.12]. Boys and Handley [5.13] analysed the equivalent SVPWM reference showing it has the form of a sinusoid injected with a triangular signal. Wu et al. [5.14] have investigated this relationship concerning a multilevel implementation.

Meynard's group at Toulouse [5.15] have used SVPWM in the control of a flying-capacitor inverter used in an induction motor drive. Voltage balancing is achieved through voltage sensors which change the switching state depending on the voltage level demand from the SVPWM algorithm. Brazilian researchers Mendes et al. [5.16] have been investigating multilevel SVPWM and have demonstrated its application to a two-cell flying-capacitor inverter. The cell-capacitor voltage balancing is achieved by monitoring the cell-capacitor voltages and phase current, and then using a simple on/off controller.

5.2.1 Three-Phase Clarke Transformation

A three-phase system of stationary reference frame voltages can be mapped to a two-phase orthogonal α-β plane. The relationship is shown in Figure 5.2.1. This is a convenient technique especially in rotating three-phase machines, since the rotating system vector in d-q axis plane is found by applying an angular phase shift. The mathematical transform for converting the stationary three-phase parameters to the orthogonal plane is known as the Clarke or Park transform.

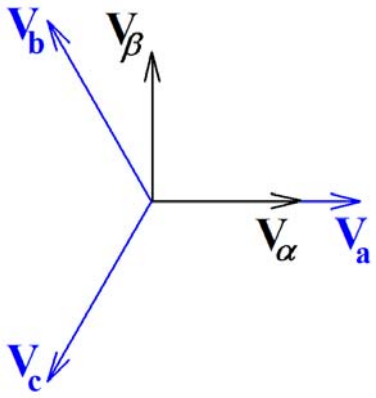

Figure 5.2.1: Relationship between stationary reference frame and complex space vector frame

The Clarke transform acts on an arbitrary set of balanced three-phase voltages to obtain the so called space vector representation in the complex α-β plane. The time-dependent vector, **V**, is derived from the individual phase voltages according to

$$\mathbf{V} = \frac{2}{3}\left(v_{an} + v_{bn} e^{j\frac{2\pi}{3}} + v_{cn} e^{j\frac{4\pi}{3}} \right) \quad \ldots (5.2.1)$$

where v_{an}, v_{bn} and v_{cn} are the stationary node voltages with respect to the centre-point neutral of a balanced three-phase load, and

$$v_{an} + v_{bn} + v_{cn} = 0 \quad \ldots (5.2.2)$$

The orthogonal reference frame components are found using

$$\mathbf{V} = v_\alpha + j v_\beta \quad \ldots (5.2.3)$$

$$v_\alpha = \frac{2}{3}\left(v_{an} + v_{bn} \cos\left(\frac{2\pi}{3}\right) + v_{cn} \cos\left(\frac{4\pi}{3}\right) \right) \quad \ldots (5.2.4)$$

$$v_\beta = \frac{2}{3}\left(v_{bn} \sin\left(\frac{2\pi}{3}\right) + v_{cn} \sin\left(\frac{4\pi}{3}\right) \right) \quad \ldots (5.2.5)$$

These simplify to

$$v_\alpha = \frac{2}{3} v_{an} - \frac{1}{3}\left(v_{bn} + v_{cn} \right) \quad \ldots (5.2.6)$$

$$v_\beta = \frac{1}{\sqrt{3}}\left(v_{bn} - v_{cn} \right) \quad \ldots (5.2.7)$$

The space vector, **V**, is also normally represented in the complex plane using

$$\mathbf{V} = V e^{j\theta} \quad \ldots (5.2.8)$$

where

$$V = \sqrt{\left(v_\alpha^2 + v_\beta^2\right)} \quad \ldots (5.2.9)$$

and

$$\theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \quad \ldots (5.2.10)$$

5.2.2 Space Vector Duty Cycle Computation

In the three-phase system, each phase voltage node can apply a voltage between $+V_{dc}/2$ and $-V_{dc}/2$. If the inverter limb circuit is a basic two-level topology, then only the minimum and maximum voltages are applied. In this case, the inverter has eight possible switching state vectors, and these form a hexagonal constellation pattern in the complex plane as shown in Figure 5.2.2. The vector identification uses a 0 to represent the negative phase voltage level and 1 to represent the positive phase voltage level.

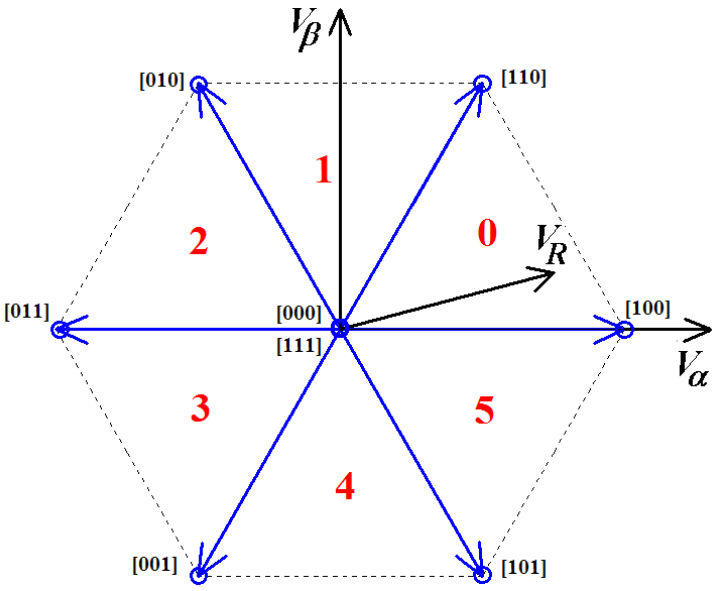

Figure 5.2.2: Inverter state space vector diagram

The duty cycle computation is done for each triangular sector formed by two state vectors. Figure 5.2.3 illustrates the vector composition required for a reference in the sector bounded by the switching state vectors [100] and [110]. The magnitude of each switching state vector is $2V_{dc}/3$. The magnitude of a vector to the mid-point of the line between each switching state vector vertex is $V_{dc}/\sqrt{3}$. The amplitude modulation index, m_a, is defined as the ratio of the peak output voltage sinusoid to maximum positive

available voltage $V_{dc}/2$. Therefore, the maximum possible modulation depth for SVPWM is 1.155 and so SVPWM can operate with modulation depths above unity, in the same way as sine-triangle PWM with 3rd order harmonic injection.

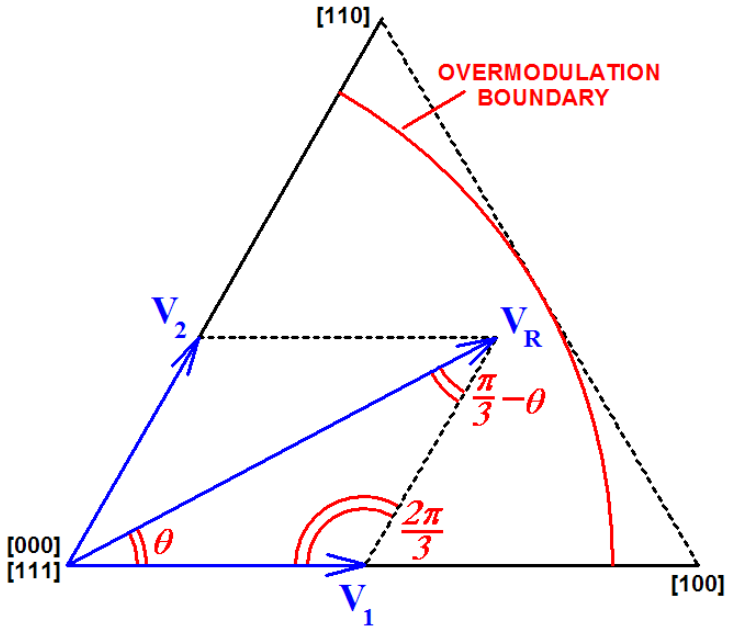

Figure 5.2.3: Sector 0 diagrammatic depiction of vector duty computation

In terms of the modulation depth, the reference vector magnitude, V_R, is given by

$$V_R = \frac{m_a V_{dc}}{2} \quad \ldots (5.2.11)$$

Therefore, the equation for the space vector computation is given by

$$\frac{V_1}{\sin\left(\frac{\pi}{3}-\theta\right)} = \frac{V_2}{\sin\theta} = \frac{m_a V_{dc}}{2\sin\left(\frac{2\pi}{3}\right)} \quad \ldots (5.2.12)$$

where

$$V_1 = D_1\left(\frac{2V_{dc}}{3}\right) \quad \ldots (5.2.13)$$

$$V_2 = D_2\left(\frac{2V_{dc}}{3}\right) \quad \ldots (5.2.14)$$

and

D_1 and D_2 are the duty cycles in one PWM switching period

So (5.2.13) can be re-written in terms of the duty cycles as

$$\frac{2D_1}{3\sin\left(\frac{\pi}{3}-\theta\right)}=\frac{2D_2}{3\sin\theta}=\frac{m_a}{2\sin\left(\frac{2\pi}{3}\right)} \quad \ldots (5.2.15)$$

Now

$$\sin\left(\frac{2\pi}{3}\right)=\frac{\sqrt{3}}{2} \quad \ldots (5.2.16)$$

Therefore, the individual duty cycles for each sector boundary state vector and the zero state vector, [000] or [111], are given by

$$D_1=\frac{\sqrt{3}}{2}m_a\sin\left(\frac{\pi}{3}-\theta\right) \quad \ldots (5.2.17)$$

$$D_2=\frac{\sqrt{3}}{2}m_a\sin\theta \quad \ldots (5.2.18)$$

$$D_0=1-D_1-D_2 \quad \ldots (5.2.19)$$

where

$$D_0=\frac{T_0}{T_s},\ D_1=\frac{T_1}{T_s}\ \text{and}\ D_2=\frac{T_2}{T_s}$$

These give switching times T_0, T_1 and T_2 for each inverter state for a total switching period of T_s. The timing diagram for SVPWM is shown in Figure 5.2.4 for the sector 0. By convention in SVPWM, the switching times are arranged as shown in the figure, so that the switching pattern is symmetric around the centre of the switching period. To do this the zero vector [111] is placed at the centre of the switching period, and the zero vector [000] at the start and end, and total period for a zero vector is divided equally amongst the two zero-vectors.

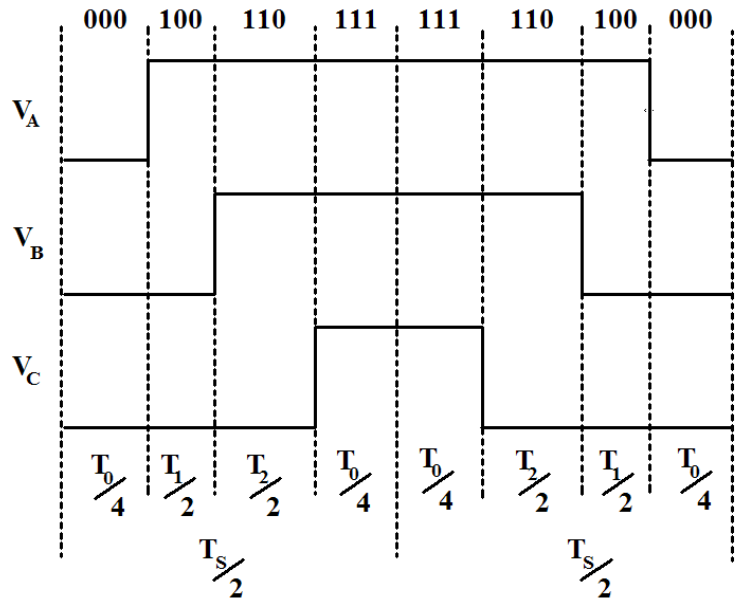

Figure 5.2.4: Space Vector Modulation Timing Diagram

In the other five sectors, the same computational process is applied. Equations (5.2.18 - 5.2.20) still apply, but the reference angle θ is offset by $-n3/\pi$, where n is the sector number, in order to reference θ to the base V_1 vector in each case. Another convention in SVPWM is to ensure there is only one switching transition within half a switching period, so the contributions of the switching state vectors are normally grouped to ensure this.

5.3 Multilevel Space Vector PWM

In multilevel inverters, the additional phase output voltage levels means that the number of state vectors is increased. In the 4-cell, 5-level inverter there are 61 distinct switching state vectors forming the constellation shown in Figure 5.3.1. The overall vector boundary still has a hexagonal form, with vertexes being the full voltage modes in each phase.

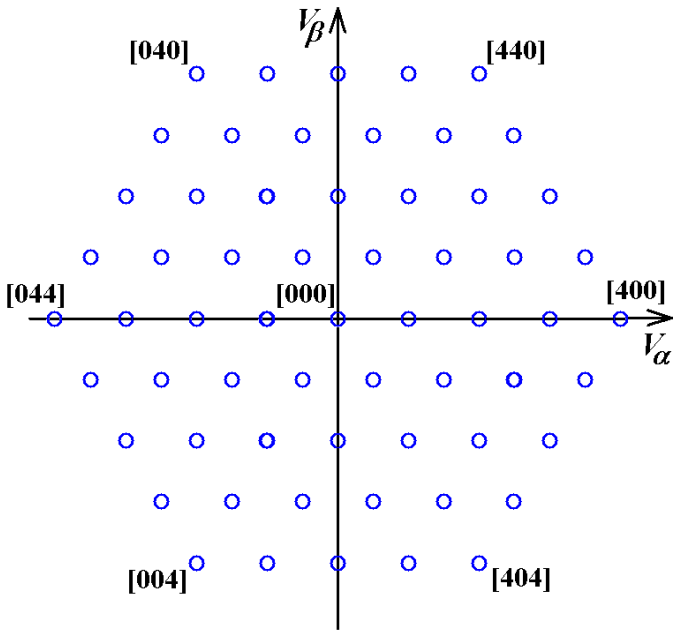

Figure 5.3.1 Four-cell inverter normalised space vector constellation diagram

The large number of possible space vectors which can be used to form a reference vector poses a computational problem. However, this complexity can be reduced to a form where the computational complexity is identical to the standard SVPWM method, and the multilevel issue of balancing can be addressed by the separate block implementation described in Chapter 4.

Figure 5.3.2 shows a reference vector together with the switching state vector points for sector 0 in the case of the four-cell inverter which has five individual phase

voltage levels. The voltage level contribution from each phase is shown in the bracketed indicator for each state vector. The reference vector is positioned within a triangle formed by state vectors [310], [300] and [410]. State vectors within the bounds of the space vector constellation hexagon can be realised with more than one switching mode. For instance, vector [310] is equivalent to [421], and the number of permutations increases towards the centre where there are 5 zero space vectors.

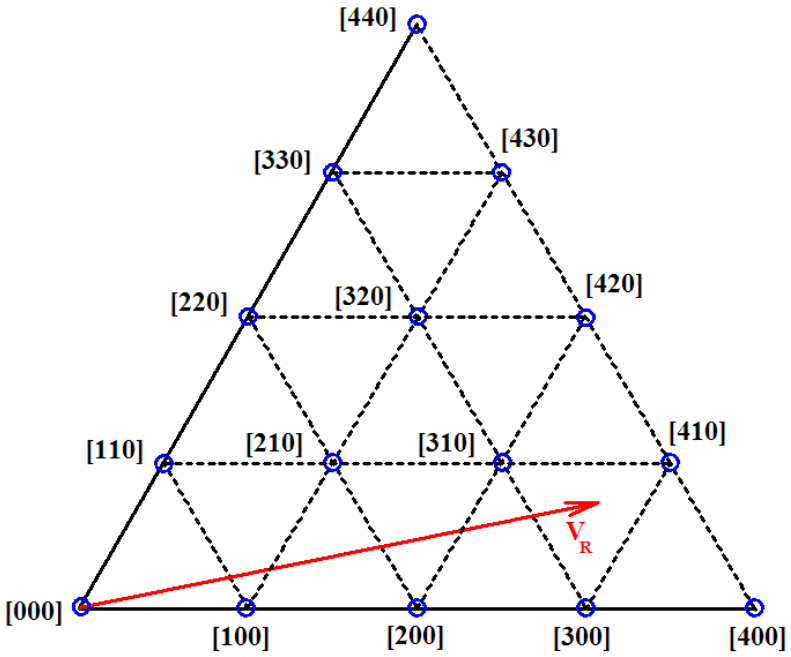

Figure 5.3.2 Voltage Reference Vector in Sector 0

The reference vector can be realised using the combination of switching state vectors shown in Figure 5.3.3. The base vector [310] represents the state of the three phases throughout the duration of the switching period. The PWM duty cycles for the additional voltage contribution can then be calculated using the triangular geometry from two vectors –[010] and [100]. The negative sign indicates that the duty cycle pulse for phase B will be subtracted from the base rather than being added.

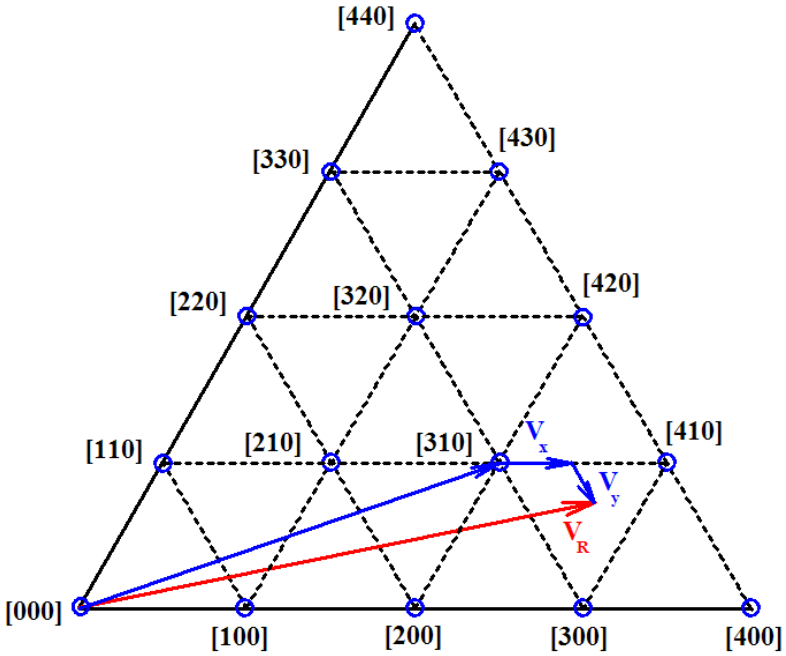

Figure 5.3.3 Vector Summation for Reference

The vector computation making up the total duty cycles for all three phases can be expressed as

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = \begin{bmatrix} 3 \\ 1 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.1)$$

The terms D_A, D_B, D_C represent the ratio of average applied voltage to maximum possible voltage (4 levels) in each phase. It is clear that the example base vector [310] can be formed using two separate vectors along the edges of the sector 0 triangle as given by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = \begin{bmatrix} 2 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.2)$$

These vectors can be further expressed as duty cycle percentages of the main hexagon vertex vectors by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = 0.5 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + 0.25 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.3)$$

Now, the relationship can be further re-arranged by introducing additional duty cycle terms for the two vertex vectors as given by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = 0.5 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + 0.25 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_{1'} \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_{2'} \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} \quad \ldots (5.3.4)$$

where

$$D_{1'} = \frac{D_x + D_y}{4} \quad \ldots (5.3.5)$$

$$D_{2'} = -\frac{D_y}{4} \quad \ldots (5.3.6)$$

This means that, mathematically, the SVPWM computation problem in a multilevel inverter can be minimised to the following form

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} \quad \ldots (5.3.7)$$

where

$$D_1 = \frac{2 + D_y + D_x}{4} \quad \ldots (5.3.8)$$

$$D_2 = \frac{1 - D_x}{4} \quad \ldots (5.3.9)$$

Figure 5.3.4 illustrates graphically the vector solutions required to obtain the reference vector in the five-level inverter.

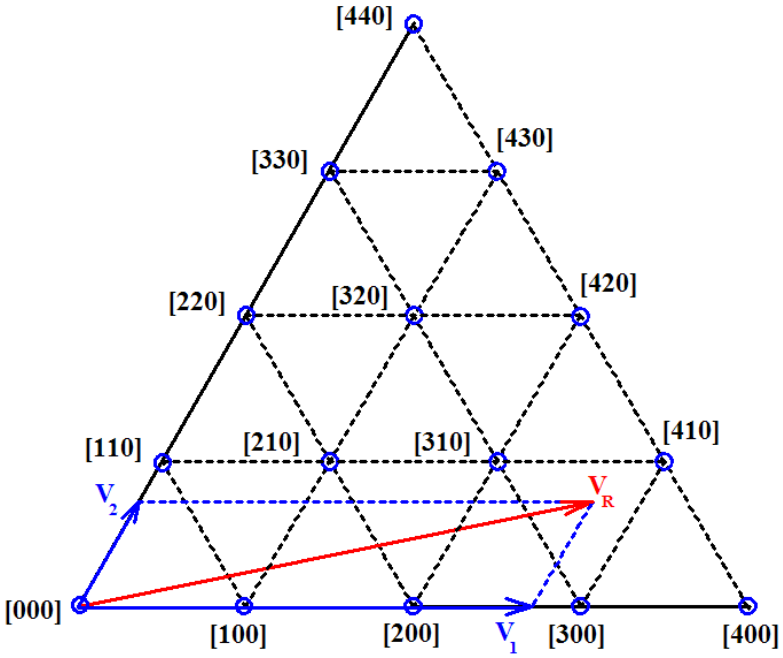

Figure 5.3.4 Space vector decomposition in sector 0

This means that the standard two-level duty cycle equations, (5.2.18 and 5.2.19) can be applied to multilevel inverters to obtain the timing information required to implement SVPWM. In the four-cell inverter, the phase duty cycle terms are first computed using the relevant sector equation, and these are listed in Table 5.3.1.

Sector, n	Phase Angle, θ	Sector Duty Equation
0	$0 \le \theta < \pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix}$
1	$\pi/3 \le \theta < 2\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 4 \\ 0 \end{bmatrix}$
2	$2\pi/3 \le \theta < \pi$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 4 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 4 \\ 4 \end{bmatrix}$
3	$\pi \le \theta < 4\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 4 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 0 \\ 4 \end{bmatrix}$
4	$4\pi/3 \le \theta < 5\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 0 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix}$
5	$5\pi/3 \le \theta < 2\pi$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix}$

Table 5.3.1: Sector duty equations

Now, these can result in phase duty cycle values greater than 1, so the results are further processed by splitting the duty cycle terms into the fractional and integer parts, to obtain the timing parameters for multilevel SVPWM control. The integer part of each phase duty cycle is the applied base voltage level over the whole switching period. The fractional part is then the ratio of the applied time for the extra voltage level added on the output to the total PWM switching period.

The base voltage level, m, for phase A in a switching cycle is the integer part of D_A. Mathematically, it is found using the floor function and is expressed as

$$m = \lfloor D_A \rfloor \qquad \ldots (5.3.10)$$

The time when level $m+1$ is applied in the centre of the switching cycle can be found from the fractional part of D_A, and is given by

$$T_{m+1} = T_s \left(D_A - \lfloor D_A \rfloor \right) \quad \ldots (5.3.11)$$

This SVPWM can be implemented in hardware using a carrier-based approach to produce the gate firing signals. The modulation timing diagrams for one phase are shown in Figure 5.3.5.

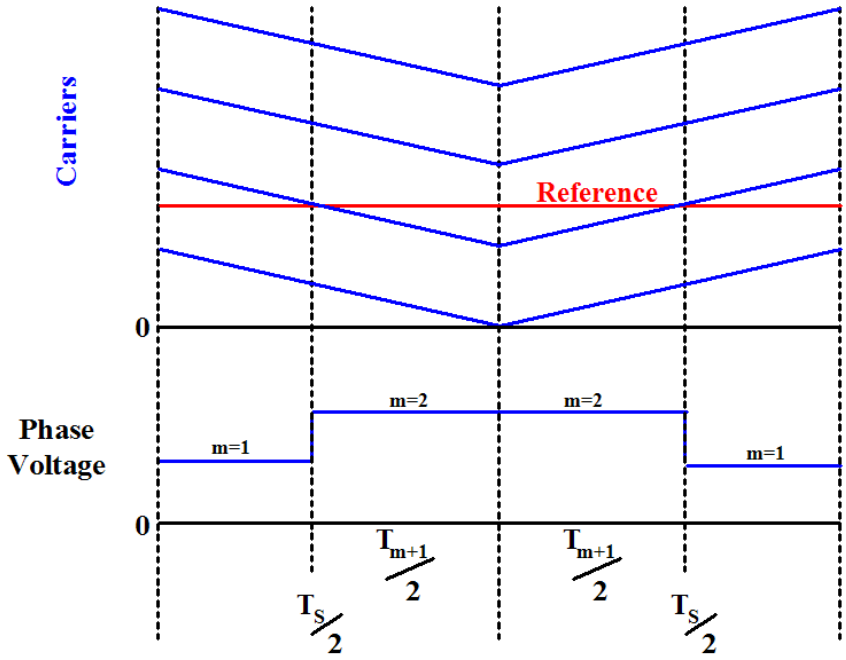

Figure 5.3.5 Space vector carrier-based implementation timing diagram

In the case of the four-cell inverter where the per unit reference span is 2, the phase reference for the comparators can be computed using the duty cycle equations,

$$D_1 = \sqrt{3} m_a \sin\left(\frac{(1-n)\pi}{3} - \theta \right) \quad \ldots (5.3.12)$$

$$D_2 = \sqrt{3} m_a \sin\left(\theta - \frac{n\pi}{3} \right) \quad \ldots (5.3.13)$$

Table 5.3.2 lists the summations required for each sector. In this case, the reference is symmetric around zero and so there is no requirement to include zero voltage vector contributions.

Sector	Phase Angle	Space Vector Phase Reference Voltages		
n	θ	V_a	V_b	V_c
0	$0 \le \theta < \pi/3$	D_1+D_2	$-D_1+D_2$	$-D_1-D_2$
1	$\pi/3 \le \theta < 2\pi/3$	D_1-D_2	D_1+D_2	$-D_1-D_2$
2	$2\pi/3 \le \theta < \pi$	$-D_1-D_2$	D_1+D_2	$-D_1+D_2$
3	$\pi \le \theta < 4\pi/3$	$-D_1-D_2$	D_1-D_2	D_1+D_2
4	$4\pi/3 \le \theta < 5\pi/3$	$-D_1+D_2$	$-D_1-D_2$	D_1+D_2
5	$5\pi/3 \le \theta < 2\pi$	D_1+D_2	$-D_1-D_2$	D_1-D_2

Table 5.3.2: Phase reference equations

The references are then applied to triangular carriers with minima at the centre of each switching period. This means that the reference must be computed and sampled at the maxima of each carrier. This is a form of symmetric regular sampling, but at the opposite points in the carrier cycle to standard carrier-based PWM schemes. The computation of the duty cycle assumes that at the minimum value all inverter cell upper switches are in the off state, so the phase disposition (PD) carrier scheme is used.

When the computed SVPWM reference is analysed, it is clear that this control method is akin to a third harmonic injection scheme. Figure 5.3.6 shows the resultant reference waveform, and its decomposition into a fundamental sinusoid plus third order triangular-shaped injected signal. Boys and Handley [5.13] analysed this triangular third harmonic component in the frequency domain, but the time domain equation can also be found.

The equivalent triangle injected waveform function, $E(\theta)$, can be found by first obtaining the peak of the decomposed pseudo-triangle injected signal at $\theta = \pi/3$. The injected waveform function for the sector where $n = 1$, is given by,

$$E(\theta) = (D_1 - D_2) - 2m_a \cos(\theta) \quad \ldots (5.3.14)$$

Expanding with the duty cycle terms gives,

$$E(\theta) = \sqrt{3}m_a\left(\sin(-\theta) - \sin\left(\theta - \frac{\pi}{3}\right)\right) - 2m_a \cos(\theta) \quad \ldots (5.3.15)$$

Now the value of E can be found for $\theta = \pi/3$ as follows,

$$E(\theta)\Big|_{\theta=\frac{\pi}{3}} = \sqrt{3}m_a\left(-\frac{\sqrt{3}}{2}\right) - 2m_a\frac{1}{2} \quad \ldots (5.3.16)$$

$$E(\theta)\Big|_{\theta=\frac{\pi}{3}} = \frac{m_a}{2} \quad \ldots (5.3.17)$$

Therefore the waveform function, *E(θ)* can be approximated to,

$$E(\theta)=\frac{m_a}{2}\left(\left(\left(\frac{6\theta}{\pi}+3\right)-2\left\lfloor\frac{3\theta}{\pi}+2\right\rfloor\right)\right)(-1)^{\left\lfloor\frac{3\theta}{\pi}+2\right\rfloor} \qquad \ldots (5.3.18)$$

There is a slight error between this triangular approximation and the actual SVPWM equivalent injected signal. Figure 5.3.7 shows the variation in the error over a whole cycle. As can be seen, the maximum error is only 0.2% and so it is possible to implement a SVPWM control using carriers and a reference composed of the summation of a sine wave and a triangular signal. This simple approach lends itself well to a digital implementation.

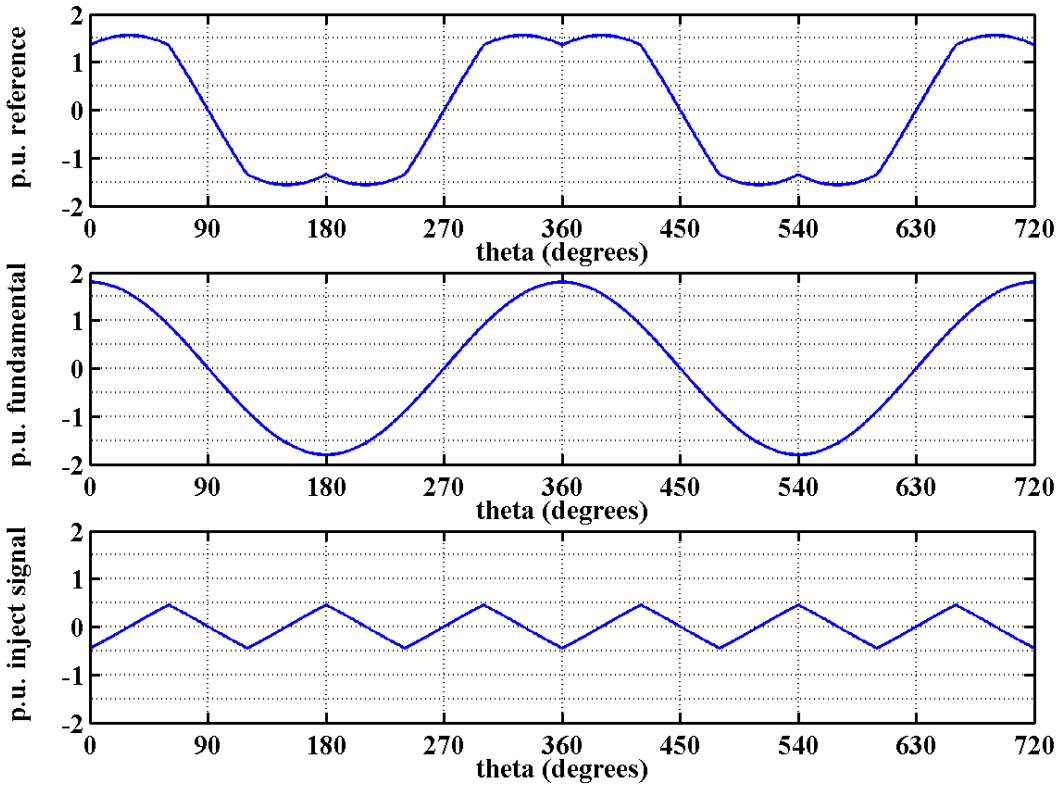

Figure 5.3.6: SVPWM equivalent reference, fundamental and injected 3rd order signal, m_a = 0.9

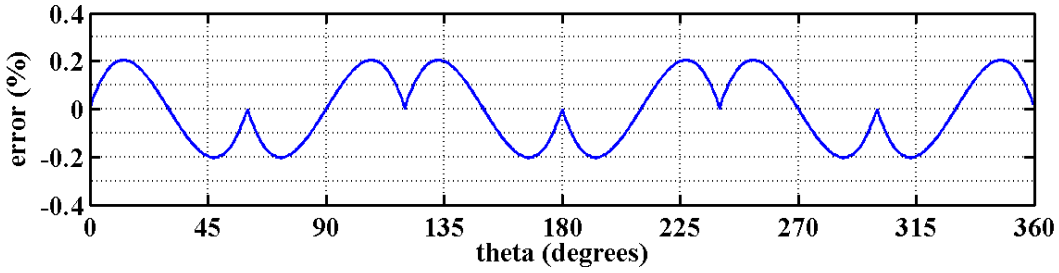

Figure 5.3.7: Error between equivalent SVPWM injected signal and approximated triangle

5.4 Ideal SVPWM Multilevel Firing Signals

This section explains some of the subtle variations in performance due to slight changes in the carrier-based implementation of the multilevel SVPWM scheme. The duty cycles are computed at the peak in the carrier waveform, and then translated into a reference signal, and this has an impact on the symmetry over a cycle of the firing signals applied to the inverter. Figure 5.4.1 shows the modulation waveforms and resultant level firing signals (no balancing algorithm) with a low modulation frequency. As can be seen, the reference is not symmetric and there will be asymmetry in the output voltage which will result in the production of odd and even order harmonics within the spectrum. This is also the case in PD PWM with symmetric sampling.

These even harmonics can be seen in the output voltage spectra shown in Figure 5.4.2. It can also be seen that the SVPWM implementation has a large harmonic at the switching frequency in the phase voltage which is cancelled in the line voltage. This spectral signature was also seen in the waveforms of sine-triangle PD PWM. The phase voltage spectrum also contains significant third and ninth harmonic components due to the injected triangular signal in the reference, which are cancelled in the three-phase load.

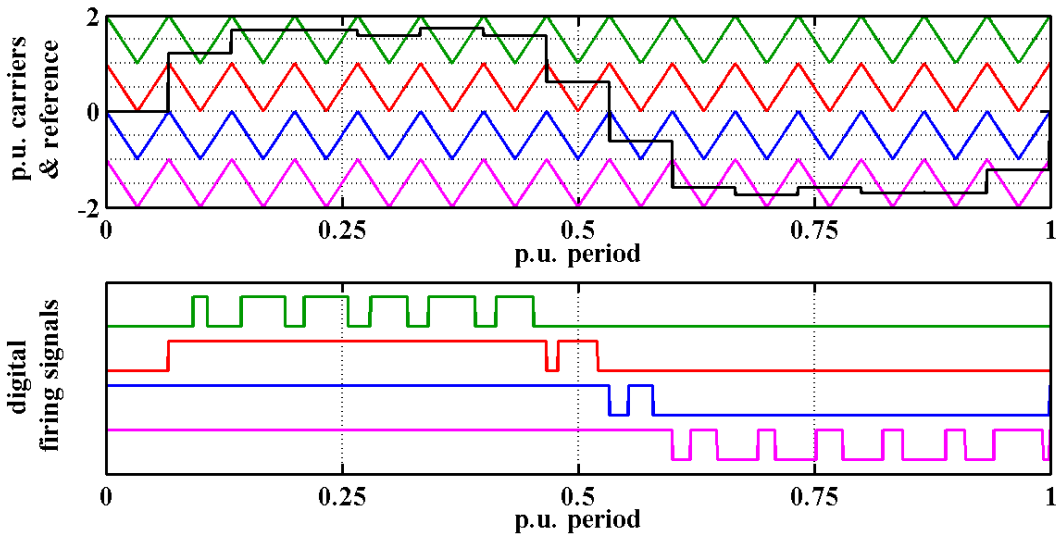

Figure 5.4.1: SVPWM waveforms, m_a = 1.0, m_f = 15

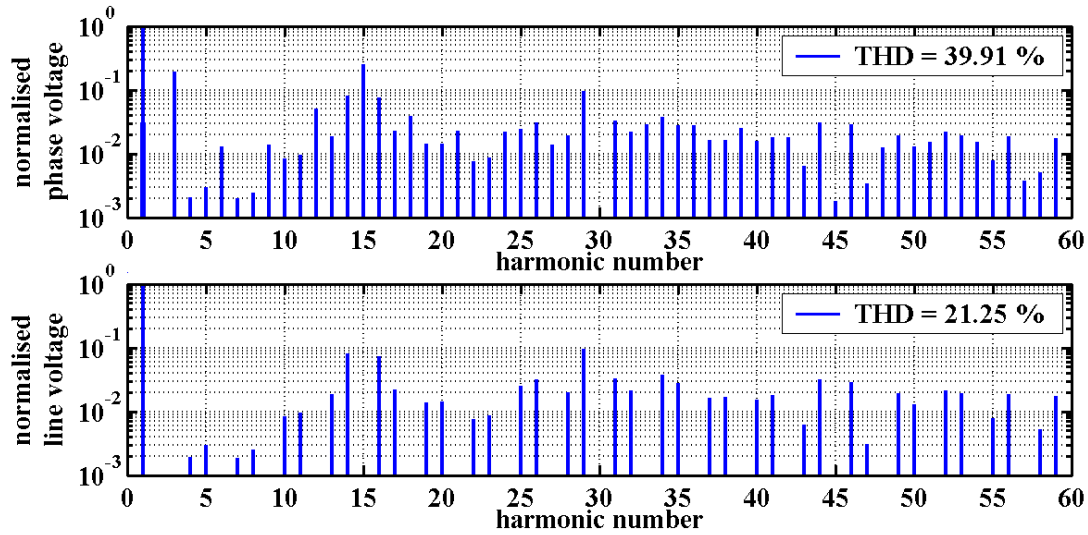

Figure 5.4.2: Voltage spectra of SVPWM, m_a = 1.0, m_f = 15

If m_f is an even number instead, then the reference will have symmetry, as shown in Figure 5.4.3. However, like the multilevel PD PWM scheme, the selection of an even m_f results in asymmetry in the output voltage. The resultant spectra, Figure 5.4.4, again include even order harmonics of the fundamental, but the overall result is very similar to the odd m_f example above.

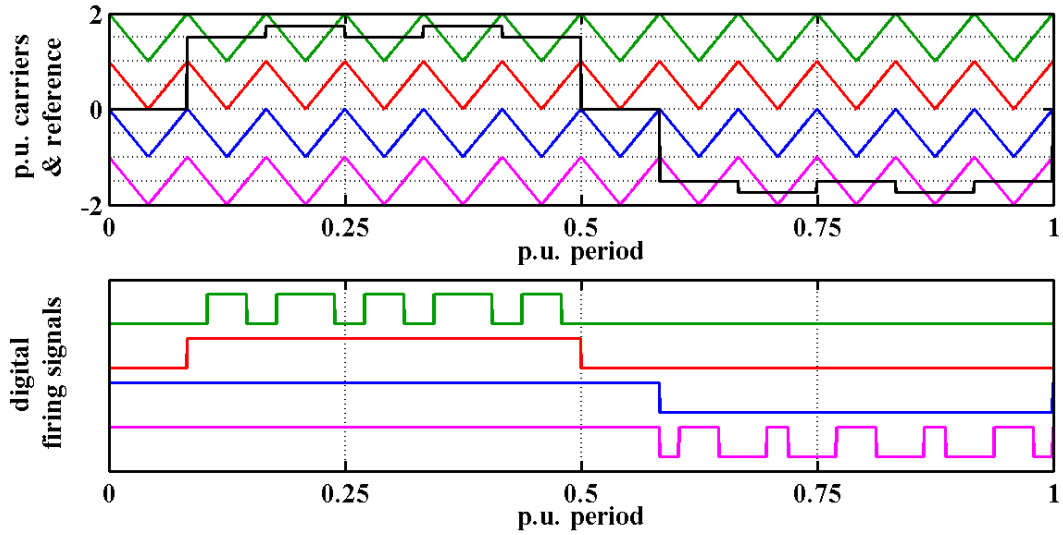

Figure 5.4.3: SVPWM waveforms, m_a = 1.0, m_f = 12

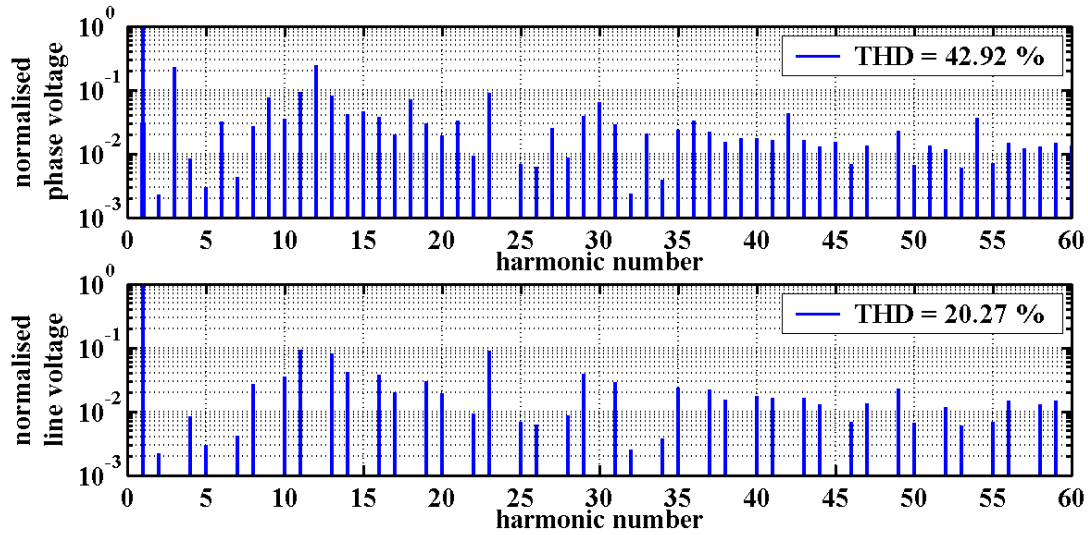

Figure 5.4.4: Voltage spectra of SVPWM, m_a = 1.0, m_f = 12

In the above example, the computation of the reference is done at each peak of the carrier, and results in a phase shift of $180/m_f$ degrees. This can be compensated for in the reference computation by adding $180/m_f$ degrees to the reference demand angle before computing the reference level. The resultant modulation waveforms are shown in Figure 5.4.5. There is still asymmetry in the output voltage as before and this leads to odd and even harmonics being present in the output voltage, as can be seen in Figure 5.4.6. Note that the THD is slightly higher than before, but this is due to the low m_f value selected.

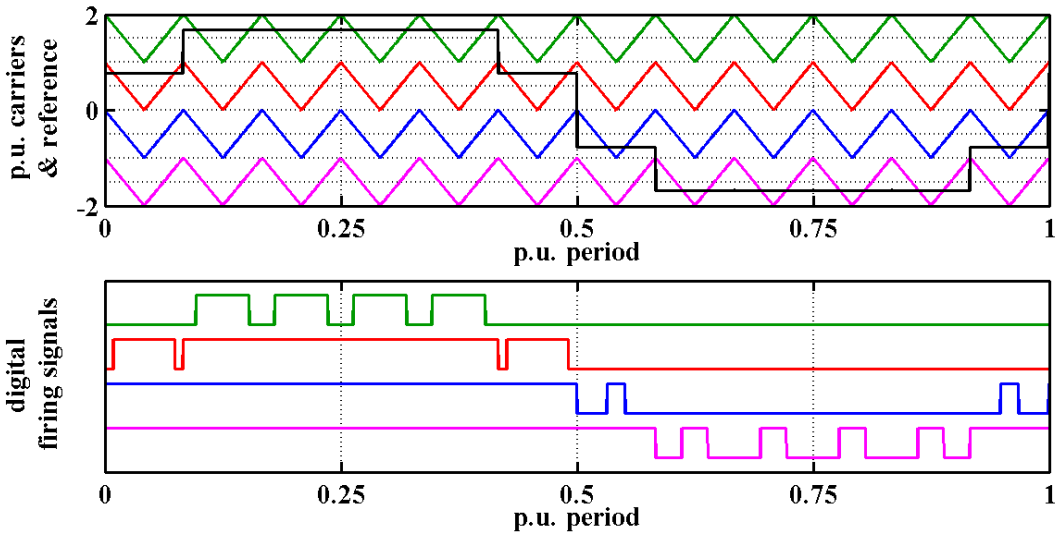

Figure 5.4.5: Phase adjusted SVPWM waveforms, m_a = 1.0, m_f = 12

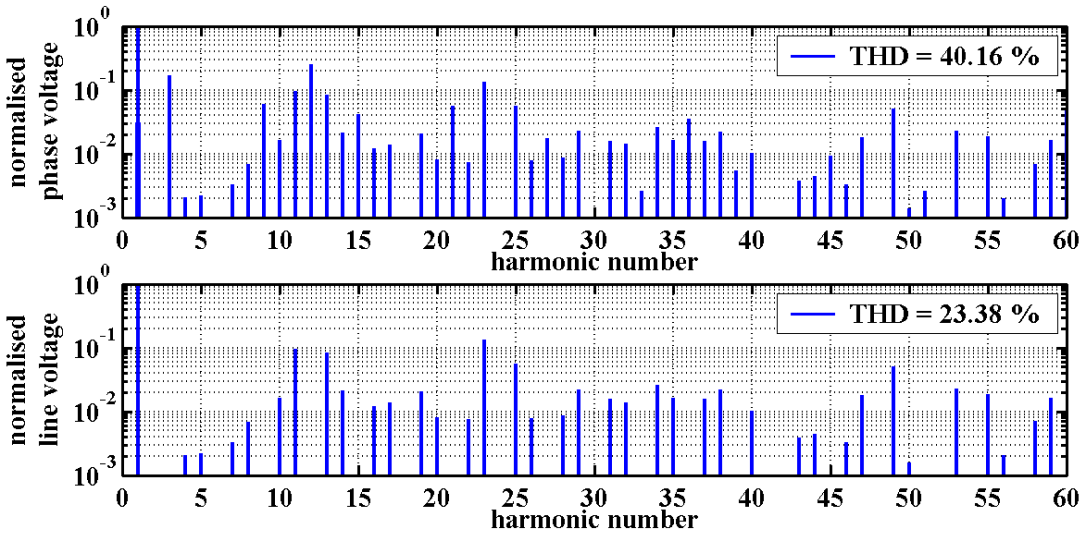

Figure 5.4.6: Voltage spectra of phase adjusted SVPWM, m_a = 1.0, m_f = 12

For higher switching frequencies, the choice of odd or even values m_f is not critical, as long as all three-phase carriers are synchronised in phase. This is because the harmonic component at the carrier frequency will only cancel in the line voltage when the carriers are in phase. This has already been shown in PD PWM. An example of the typical voltage spectra at a high m_f is shown in Figure 5.4.7. The overall performance of this SVPWM implementation under the ideal conditions of no cell-capacitor voltage variation is very good as can be seen by the relatively low line voltage THD. The output quality performance is very similar to that seen for PD PWM.

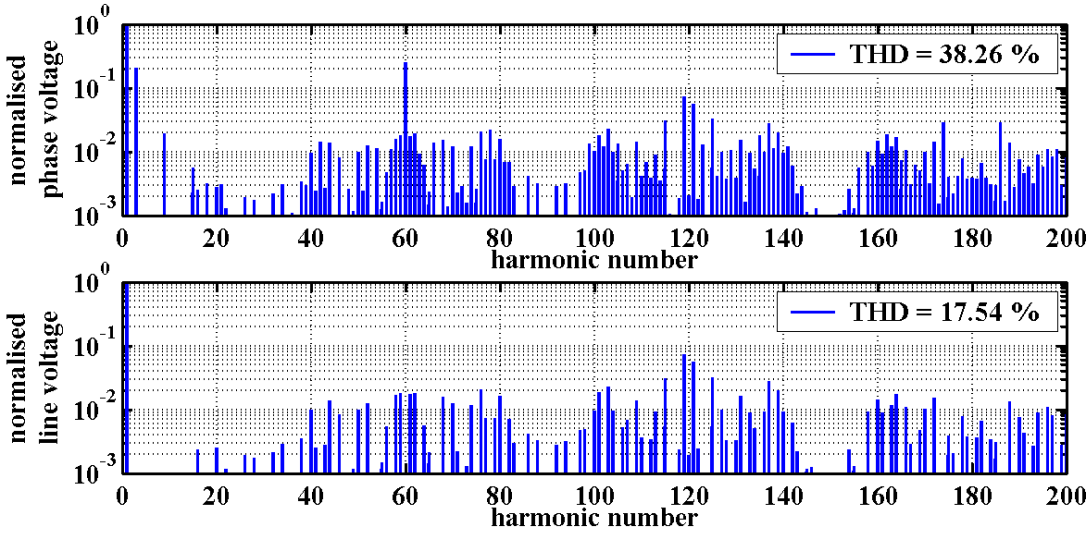

Figure 5.4.7: Voltage spectra of SVPWM with angle adjust, m_a = 0.9, m_f = 60

The phase-shifting of the reference computation to take into account the sampling delay of the carriers is the preferred implementation of the SVPWM scheme which

will be used throughout the analysis of the flying-capacitor simulated inverter. Figure 5.4.8 shows the variation in THD as a function of modulation depth for a perfectly balanced system with m_f = 60. Figure 5.4.9 shows the variation in computed DF1 under the same conditions. These curve show that low harmonic distortion achievable over a wide output voltage amplitude operating range, and are very similar to the ideal characteristics of the sine-triangle PD PWM scheme presented in the previous chapter.

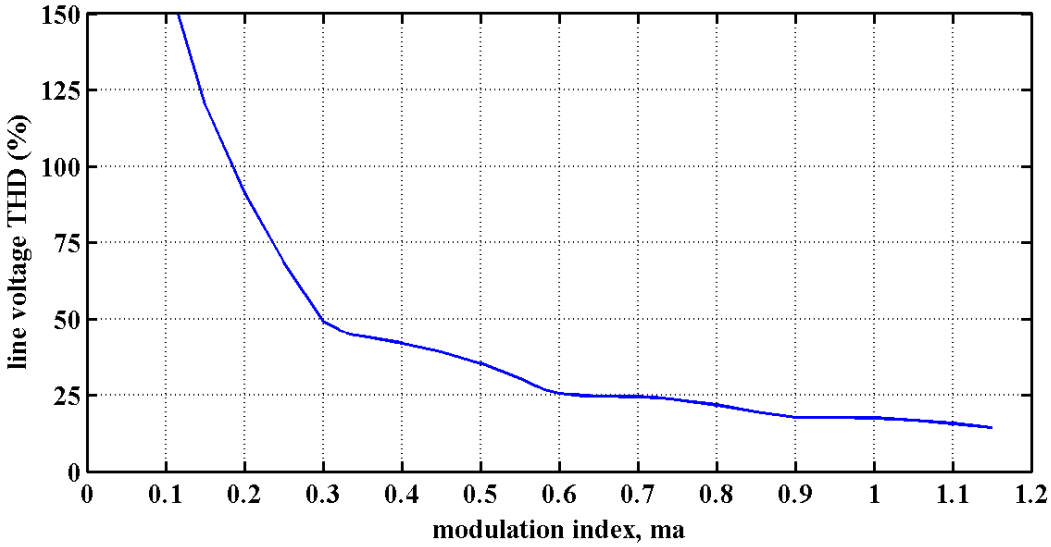

Figure 5.4.8: THD versus modulation index, m_a for SVPWM with m_f = 60

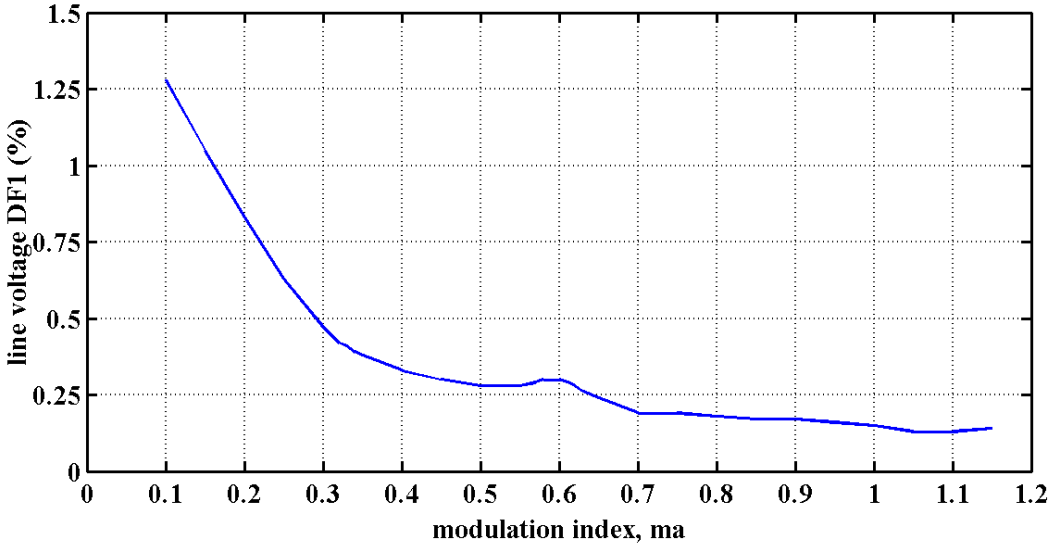

Figure 5.4.9: DF1 versus modulation index, m_a for SVPWM with m_f = 60

5.5 Performance of Balanced Inverter

The implementation of the SVPWM scheme is eminently suitable for applying the sub-carrier balancing scheme developed for sine-triangle PWM and presented in Chapter 4. For a direct comparison between the two types of PWM generation, the flying-capacitor inverter simulation uses the same modulation settings and load model used in Chapter 4. The inverter operates from a 400 V dc link and the unit cell-capacitance is 1 mF. The three-phase generic load model parameters are R_G = 0.5 Ω, L_G = 4 mH, P = 3.75 kW with DPF = 0.8. The control settings are 3 kHz switching frequency (m_f = 60), unity modulation depth (m_a = 1) and 3 μs dead-time.

Figure 5.5.1 shows the operating waveforms for the inverter controlled using the SVPWM scheme. The capacitor voltages are well balanced with only a small voltage ripple, and the phase currents exhibit low harmonic distortion. The load star point voltage waveform contains a dominant triangular shaped ripple component which is due to the effective injected signal in the equivalent reference of the SVPWM scheme.

Figure 5.5.2 shows the spectra of the inverter output waveforms. Both the switching frequency component and the third order harmonic are clearly visible in the phase voltage spectrum, but are cancelled in the three-phase load as can be seen in the line voltage spectrum. The spectral hump below 1 kHz seen in both the line voltage and phase current spectra is due to the voltage ripple in the cell-capacitors, and contributes in an increased THD above the ideal level.

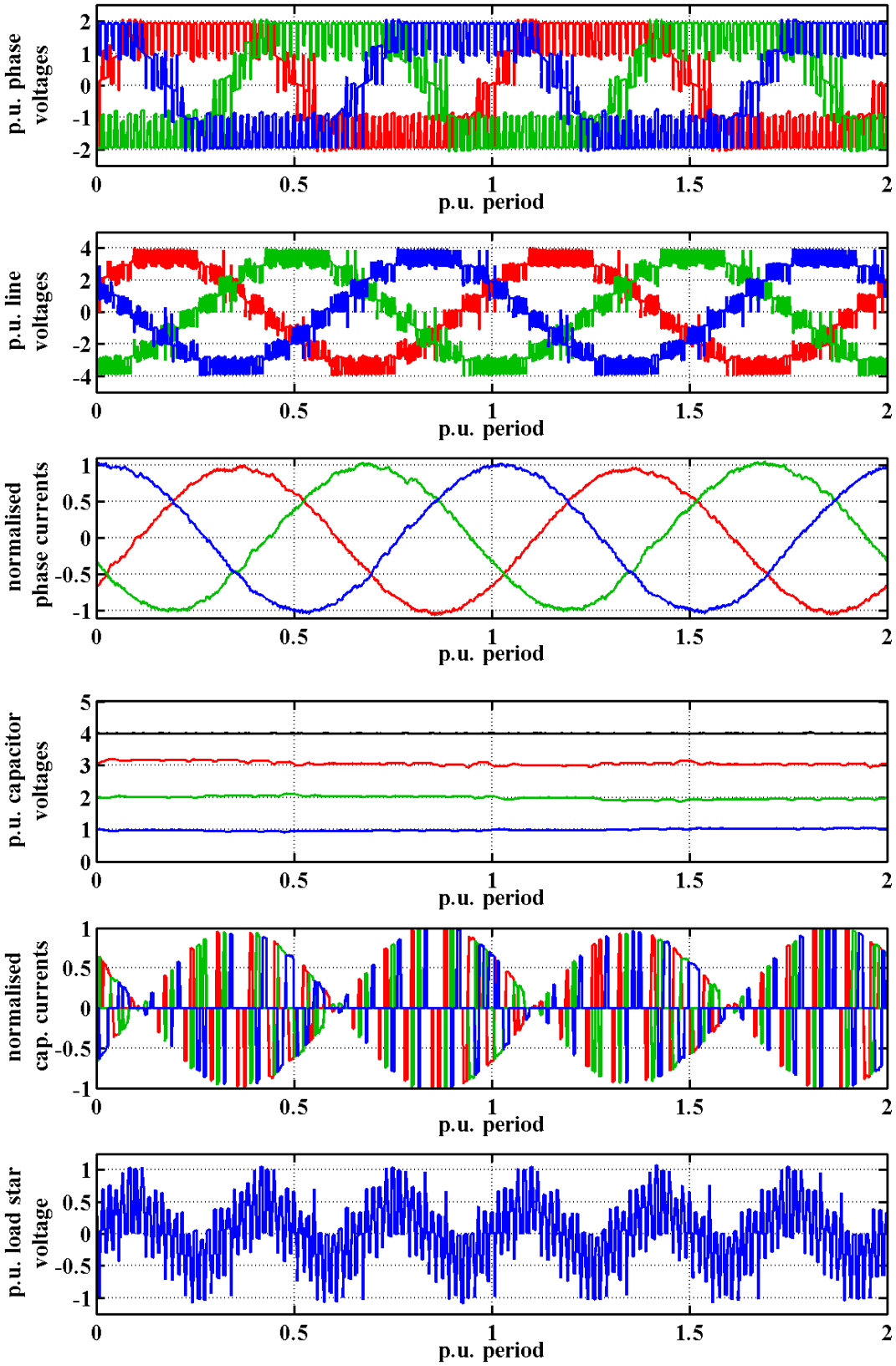

Figure 5.5.1: SVPWM waveforms, m_f = 60, m_a = 1.0

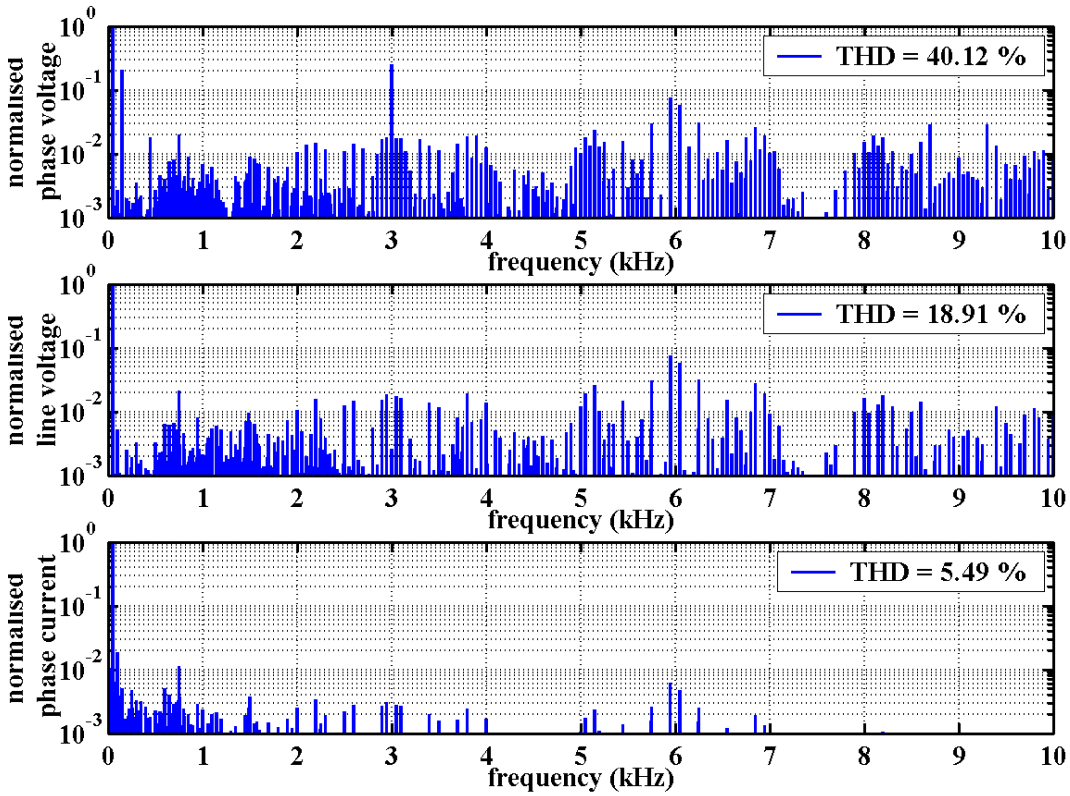

Figure 5.5.2: SVPWM spectra, m_f = 60, m_a = 1.0

The results can be compared with third-harmonic injected sine-triangle scheme, which also allows for increased modulation depth above unity. Table 5.5.1 lists the simulation results for the two schemes operating at two different modulation depths. As can be seen, there is very little to choose between these two control methods.

Scheme	m_a	Phase Voltage (Vrms)	Phase Current (Arms)	Line Voltage (Vrms)	TPF	Power (kW)	Loss (W)
SVPWM (m_a = 1.0)	0.97	147.7	11.5	242.0	0.76	3.84	188
PD + 1/6th (m_a = 1.0)	0.97	146.7	11.3	241.9	0.74	3.70	186
SVPWM (m_a = 1.1)	1.07	160.1	10.3	266.3	0.76	3.76	166
PD + 1/6th (m_a = 1.1)	1.07	158.9	10.2	266.6	0.76	3.68	163

Table 5.5.1: Output performance comparison of different schemes

Table 5.5.2 lists the total harmonic distortion factors for the two control modes. Here there is a slight improvement in phase current quality for the sine-triangle case. This is because the additional harmonics introduced by the effective reference of the SVPWM method, introduces additional inter-modulation harmonic products due to the cell-capacitor voltage frequency components.

Scheme	Phase Voltage THD (%)	Line Voltage THD (%)	Phase Current THD (%)
SVPWM (m_a = 1.0)	40.12	18.91	5.49
PD + 1/6th (m_a = 1.0)	37.33	18.63	4.43
SVPWM (m_a = 1.1)	34.15	16.67	4.42
PD + 1/6th (m_a = 1.1)	30.89	16.68	4.11

Table 5.5.2: Output distortion comparison of different carrier schemes

Table 5.5.3 compares the capacitor and power switch operating parameters and shows that both systems are well balanced although there is a slight increase in capacitor ripple voltage for the sine-triangle case. This means that the power devices must withstand around a 5 % higher blocking voltage in the third harmonic injected sine-triangle PWM case. However, this reduced capacitor voltage ripple amplitude in the SVPWM case does not translate into lower THD for the phase current waveform.

Overall, the performance of the two schemes is very similar, and the choice between which control strategy suites the application best will be based on the hardware implementation. The SVPWM requires greater computational effort in order to generate the duty-cycle reference and so a DSP implementation may be needed. However, it is possible to pre-compute a reference, and adjust the amplitude in real-time based on the amplitude modulation index. This means that both schemes can be implemented in almost identical digital hardware.

Scheme	Cell-Capacitor Voltages (V)			Max. Switch (V)	Cap. Current (Arms)	Peak Power Loss		
						IGBT (W)	Diode (W)	Trans. (W)
SVPWM (m_a = 1.0)	99.2	198.0	301.8	124.8	5.59	6.60	1.42	0.16
PD + 1/6th (m_a = 1.0)	102.1	200.5	301.4	130.9	5.57	6.42	1.36	0.16
SVPWM (m_a = 1.1)	99.9	199.9	300.0	120.4	4.26	6.07	1.02	0.15
PD+ 1/6th (m_a = 1.1)	101.5	200.3	300.3	124.7	4.27	5.87	0.99	0.14

Table 5.5.3: Phase balancing performance comparison of different carrier schemes

5.6 Conclusions

It has been shown that the space vector PWM scheme can be implemented in a very simple manner even for complex systems like the multilevel flying-capacitor inverter. The relationship that exists between the standard SVPWM and sine-triangle, carrier-based PWM was exploited to simplify the multilevel SVPWM duty-cycle computation rather than using a more complex algorithm based on the sub-sector triangles reported by other researchers.

The sub-carrier balancing implementation developed for cell-capacitor voltage ripple minimisation when controlled using sine-triangle PWM also functions correctly when used in SVPWM control. This means that the flying-capacitor SVPWM algorithm is simplified since it does not need to consider the actual switching states, and only operates on the voltage level vectors.

The simulated performance is on a par with optimised sine-triangle schemes, and results have been presented of SVPWM operation including a greater than unity modulation depth. SVPWM performance has been compared to third harmonic injection sine-triangle PWM and the results show the similarity between the two schemes.

5.7 References

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