Chapter 2 CONVERTER MODELLING AND ANALYSIS

2.1 Introduction

The flying-capacitor multilevel converter, the subject of this thesis, was first proposed by Meynard and Foch in 1991 [2.1]. In this chapter the existing knowledge on the circuit and its' applications are reviewed through the published literature. Later sections then explain the circuit operation and address the necessity to balance the cell-capacitor voltages. A simple matrix model is developed to provide a means for basic circuit modelling and as a tool for further circuit analysis. Options for more advanced simulation of the circuit, especially for investigating the effect of the capacitor voltage variations on performance, are explored in later sections. Finally, the inverter simulator program specifically developed for this research work is described. The generic load model and power quality definitions used throughout the simulation and experimental work for comparative appraisal of different modulation and system balancing control strategies are also introduced. A new parameter is also proposed for assessing the performance of an inverter design based on the rating of the cell-capacitors and the amount of energy stored in the inverter.

2.2 Review of State-of-the-Art

In comparison with other multilevel converter circuits, the flying-capacitor topology has received less attention since its first disclosure in the early 1990s. In total, 153 papers have been identified as being specifically related to the flying-capacitor converter topology and published up until 2004. Of these, around 40% are linked directly to the work of Meynard et al. at the Institut National Polytechnique de Toulouse, France. Figure 2.2.1 shows the number of papers published globally in journals and conferences since 1992. The total number of papers includes 46 English and 16 non-English language journal papers. As can be seen, interest in the topology from other researchers has only happened relatively recently, but the level of publications is still quite low. In comparison there have been at least 206 papers published on other multilevel inverters in 2004 alone.

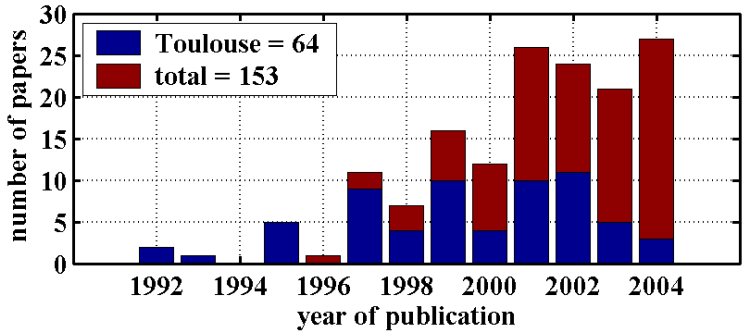


Figure 2.2.1: Annual flying-capacitor paper publication rate

The Toulouse group's progress in developing the flying-capacitor circuit in both chopper and inverter can also charted through the patents filed over the intervening period since their first disclosure [2.1]. There have been 11 individual patent filings and their main industrial collaborators, the Alstom group of companies, are the principal beneficiaries of the intellectual property rights. The implications of this are that other companies seeking to commercialise the flying-capacitor converter will probably need to obtain licensing rights before 2010 at the very least. This is the most likely reason why the amount research on the flying-capacitor converter topology around the globe has been low.

The significant amount of academic literature published by the Toulouse group has covered various aspects of the flying-capacitor topology. Their work initially focussed on the circuit's basic operation, especially as a chopper [2.2, 2.3], and led to the development of the 3 kV to 1.5 kV three-cell GTO chopper for the Alstom T13 locomotive, 80 of which now operate on European railways [2.4]. The extension of the capacitor-clamping concept to inverters was also reported at an early stage [2.5, 2.6], and work has been reported on inverter limbs with eight levels [2.7].

The inherent self-balancing capability of the circuit was understood from an early stage [2.8], although a fuzzy logic controller to improve closed-loop capacitor voltage balanced was later developed [2.9]. Significant work, initially on modelling the capacitor voltages variations [2.10], has led to the development of voltage observers for use in active cell-capacitor voltage regulation [2.11]. A phase-shifted carrier PWM control strategy has been favoured by the group for modulating the output voltage of the flying-capacitor inverter in most papers [2.12], and no work has been reported on alternative modulator control strategies.

The more recent work has led to the extension of the cell concept to a wide variety of derived multi-cell topologies. The so-called stacked multicell converter [2.13] combine two standard inverter limbs together, sharing one set of series connected switches, with cell-capacitors arranged in between the switches. Figure 2.2.2 shows an

example of the stacked multicell. Note that the current is blocked from flowing when both switches are off in the common centre limb. These topologies give increased numbers of voltage levels, and reduce the size of the capacitors, as an alternative to simply increasing the number of cells in the standard flying-capacitor inverter. Other derived topologies investigated include various quasi-resonant, soft-switching converters [2.14]. Another important issue regarding the power converter stage investigated by the group has been failure modes of different parts of the circuit and remedial control techniques for fault-tolerance [2.15, 2.16].

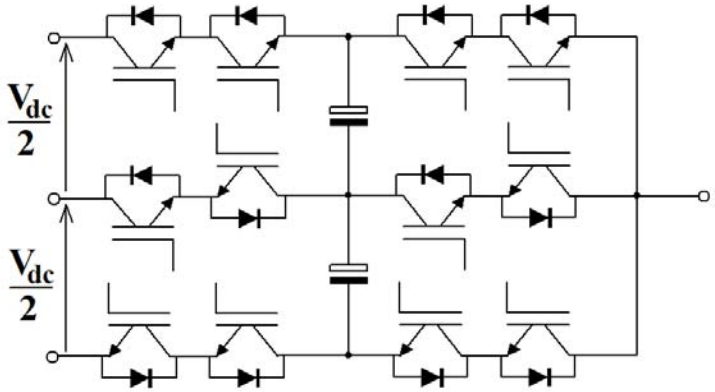


Figure 2.2.2: Stacked multicell converter circuit

In terms of applications areas, the Toulouse group have investigated a direct torque controlled (DTC) induction motor drive [2.17] and active harmonics filtering [2.18]. Meynard has also collaborated with researchers in Canada on an uninterruptible power supply (UPS) [2.19]. He also collaborated with researchers at Stellenbosch who have been investigating the flying-capacitor inverter for a number of years [2.20, 2.21].

There has been some significant work reported by researchers from other institutions. Of significance is the work at Grenoble on a sliding mode capacitor voltage control (CVC) algorithm, which has been shown to improve the dynamic performance of the inverter in an induction motor application [2.22, 2.23]. Researchers at Eindhoven, have investigated capacitor voltage balancing using system modelling [2.24] and have developed detailed analytical models for calculating the losses in the cell-capacitors to aid practical inverter design [2.25].

In respect to control strategies, specific research on the flying-capacitor inverter is sparse. However, other multilevel inverter modulation schemes described in the literature can also be applied to the flying-capacitor inverter in conjunction with a relevant capacitor voltage balancing strategy. Researchers at Hanyang University have investigated carrier rotation for multi-carrier PWM schemes and reported the

balancing properties when applied to the flying-capacitor inverter [2.26, 2.27]. Researchers at Zhejiang University have developed a carrier scheme which varies the triangular carrier amplitude in order to balance through firing rotation [2.28]. They have also investigated the relationships between PWM control and switching loss [2.29].

Agelidis et al., at the University of Glasgow have investigated the flying-capacitor inverter under phase shifted PWM control. They have simulated a novel balancing scheme which uses an injected small square wave in the reference [2.30]. The target application of this work is for high voltage ac power conditioning systems such as a unified power flow controller [2.31].

Researchers at Tsinghua University have recently published their work on a simplified PWM algorithm which incorporates rule based firing rotation for balancing and claims to give similar performance to a space vector algorithm [2.32]. Space vector modulation itself has been investigated for the flying-capacitor inverter by Mendes et al. [2.33]. They have developed a space vector algorithm for multilevel inverters in general, and achieve capacitor voltage balancing independently of the modulator by separately sensing the capacitor voltages and currents, and adjusting the inverter firing accordingly.

Researchers at Queensland University [2.34] have developed a hysteresis current controller which they implemented in an FPGA and used to control a flying-capacitor inverter. Like Mendes, they have used voltage and current sensing with a rule-based controller to achieved balancing.

Some work has been undertaken at the Swiss Federal Institute of Technology on a soft-switching three-level inverter, which uses additional circuitry for forming a resonant circuitry to ensure zero-voltage switching in the main power devices [2.35]. By controlling the four addition power switches, the clamping capacitor voltage is balanced. They have also done some detailed analytical work on the self-balancing mechanism [2.36]. Song researching at Virginia Tech. has also performed a detailed investigation on soft-switching flying-capacitor topologies targeted at active power filtering applications, and has developed rule based capacitor voltage balancing strategies for these systems [2.37].

Workers at Wisconsin University have investigated fault tolerance in the flying-capacitor inverter, and analysed the behaviour under different switch failures and the resultant effect on output voltage level and distortion [2.38]. There work assumes that the system voltages are all balanced.

Other work reported on capacitor voltage balancing include SUPERLEC team's investigation on capacitor voltage balancing using voltage sensing and a hysteresis

band controller [2.39]. Researchers at Lille have also investigated voltage balancing but focussed more on modelling the behaviour of the circuit. [2.40].

National Yunlin University investigators have been researching active front-end rectifiers and power factor correction, and have published a significant number of papers on this subject over the last four years [2.41, 2.42].

Commercially, very little has been reported on real application development although, workers at Alstom (USA) have investigated a power line conditioner application [2.43]. Developers at Alstom (Germany) described the SYMPHONY drive family which are designed for induction motors up to power ratings of 3000 HP [2.44]. They also presented possible application areas for the drive system including large off-shore wind turbine generators. Another paper from Alstom (Germany) reported on control techniques which adjusts the control for balancing purposes depending on the difference in voltage between two adjacent cell-capacitors [2.45]. The Alstom group have the rights to the original patents on the flying-capacitor converter, and have filed a group of patents with respect to the chopper circuit for the T13 locomotive [2.46].

ABB (Sweden) have also been investigating the commercial application of the inverter in power conditioning systems, and they have filed a number of patents on the balancing control of the inverter [2.47].

In a departure from the conventional applications of the flying-capacitor converter topology, researchers at Xi'an Jiaotong University have proposed a multilevel matrix converter [2.48], which uses a two-cell converter arrangement in place of a single bi-directional switch, and with the flying capacitors operating with ac voltage rather than dc.

Overall, there has been no work published specifically on flying-capacitor inverter control optimisation for sinusoidal voltage generation using staircase (selective harmonic elimination). Although various PWM control strategies have been adopted by different research groups, there has been no in depth comparative analysis of the various multi-carrier PWM techniques. The effects of cell-capacitor voltage variation on performance and the trade-offs between control strategies and capacitor size is another area where no significant work can be found in the public domain. These issues are of practical importance in future flying-capacitor inverter commercial development, and it is these areas where the work reported in this thesis is primarily focussed.

2.3 Fundamental Circuit Operation

2.3.1 Flying-Capacitor Converter Topologies

The basic building block of any power converter circuit is the chopper module, where a source dc voltage supply is sequentially connected on and off to an output circuit, and together with additional circuitry forms a power converter. There are two forms of power circuit module for the three-level flying-capacitor chopper topology. These chopper circuits operate with only unidirectional current flow and can be configured as dc-dc converter circuits with the addition of inductors and capacitors in the same way as conventional single-switch, switch-mode regulators. Figure 2.3.1 shows the high-side module in a step-down, buck regulator circuit, and Figure 2.3.2 shows the low-side module in a step-up, boost regulator circuit. Other potential applications include single-quadrant adjustable speed dc motor drives and regenerative energy dumps in other motor drive systems.

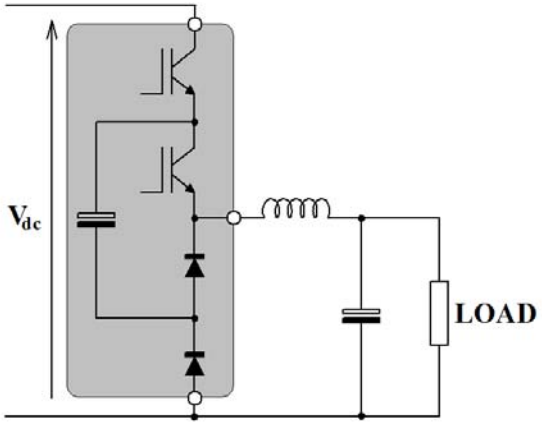


Figure 2.3.1: Buck regulator using high-side chopper module

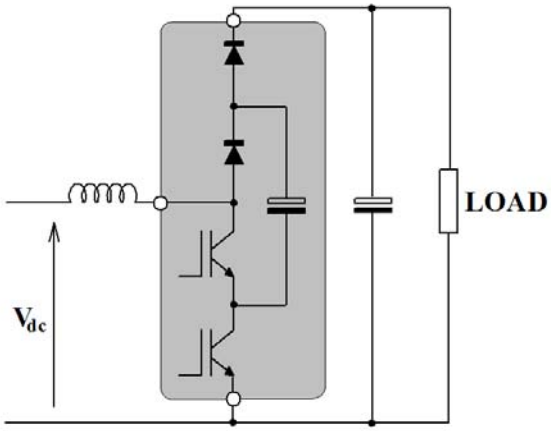


Figure 2.3.2: Boost regulator using low-side chopper module

By combining the two chopper module circuits, bridge circuits can be realised. Three basic forms of bridge circuit can be realised using the three-level chopper modules. Figure 2.3.3 shows the asymmetric bridge consisting of a single high- and low-side chopper. The load current is unidirectional, and so this topology is only suitable for forward converter switched-mode power supplies and switched reluctance machine drives [2.49]. Bidirectional load current flow is achieved by paralleling a high- and low-side chopper, to form a bridge inverter limb. Figure 2.3.4 illustrates the half-bridge topology while Figure 2.3.5 illustrates the full-bridge topology. The inverter bridge can be further extended to multi-phase circuits; most significantly for the majority of application requirements, the three-phase bridge.

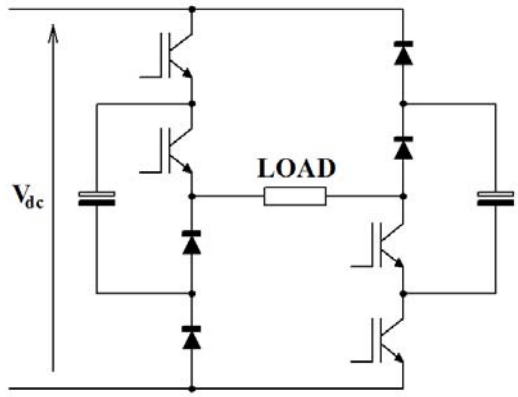


Figure 2.3.3: Asymmetric bridge circuit

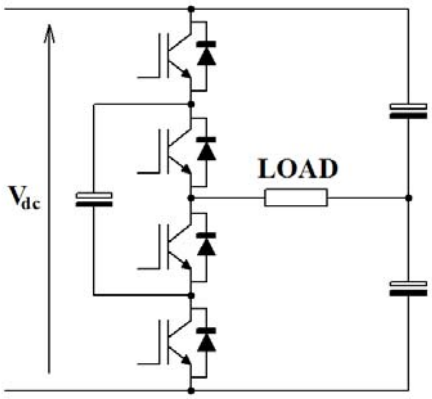


Figure 2.3.4: Half-bridge circuit

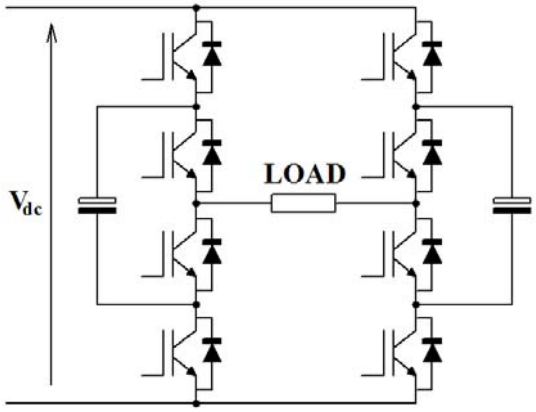


Figure 2.3.5: Full-bridge circuit

The flying-capacitor topology can be easily extended to more voltage levels by adding additional switch pairs and a capacitor. An inverter limb is in the form of a series of connected cells nested inwardly toward the load from the dc link. Figure 2.3.6 illustrates the three-cell configuration. Each cell, as shown in the figure, is composed of a capacitor and two power switches, with the outer cell being the dc link capacitor, not shown. These switches require bidirectional current paths, of which one path is controlled, for example using an IGBT with an anti-parallel diode. Each of the two cell power transistors are operated in a complementary manner. By convention, the cell-capacitors are shown as multiples of a single unit cell-capacitance, indicating the increasing voltage across each capacitor for cells nearer the high-voltage, dc link.

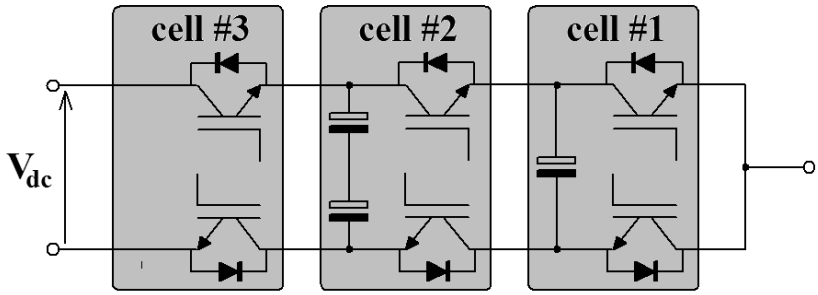


Figure 2.3.6: Four-level inverter limb

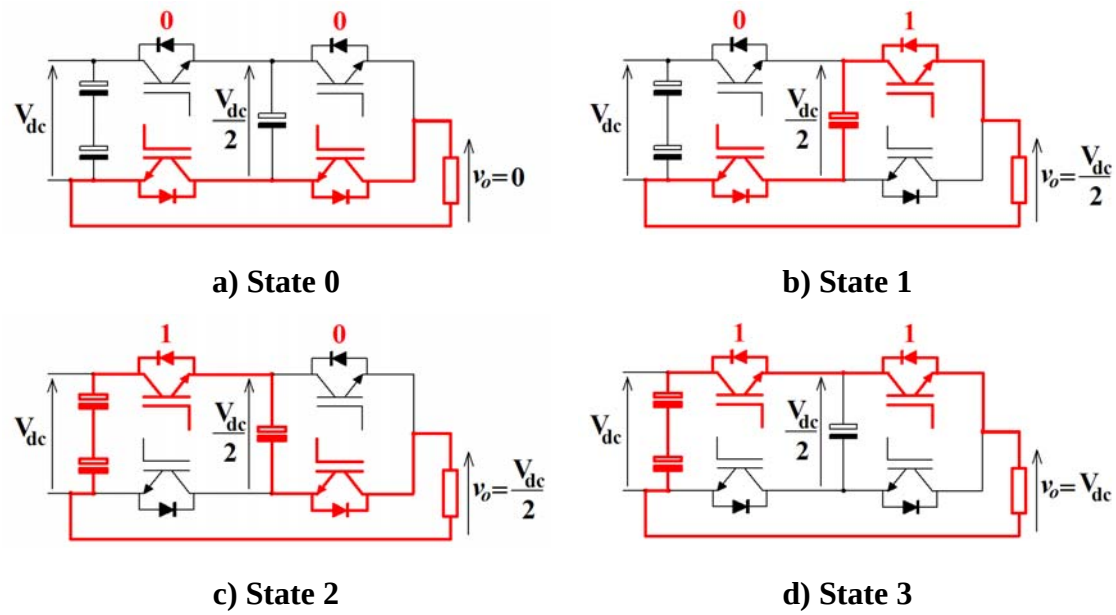
The number of voltage levels in the flying-capacitor inverter is a function of the number of complementary switch pair cells. An *N*-cell inverter limb has *2N* switches and can provide *N+1* distinct dc voltage levels from zero to V_{dc} at the load terminal with respect to the negative dc link voltage. When two limbs are configured as an inverter bridge, then there can be *2N+1* distinct voltage levels across the load

terminals. In a balanced inverter, the floating cell-capacitor average voltages are ideally kept at multiples of V_{dc}/N. Therefore, the cell-capacitor voltages will range between V_{dc}/N and $(N-1)V_{dc}/N$, with the lowest voltage across the capacitor associated with the complementary switch pair nearest the load terminal.

2.3.2 Inverter Operating States

The flying-capacitor inverter limb is controlled by operating all the complementary switch pairs so that either a high- or low-side transistor is commutated in each cell. If both switches are turned-on then this will lead to failure since it constitutes a shoot-though in the load connected cell or an unconstrained current path between a higher voltage capacitor and a lower voltage capacitor in the other cells. When both switches in a cell are not driven on, which is the case when dead-times are introduced to avoid shoot-through between cell state changes, then the polarity of load current flowing at the lower capacitor terminals will dictate which path the current will take via one of the anti-parallel diodes.

In the case of the basic two-cell inverter limb, there are four possible switching states (cell conduction states). Figure 2.3.7 shows the four current conduction paths for a load connected to the negative dc link terminal. As can be seen, there are two ways in which the half-voltage level can be applied to the output terminal. The highest and lowest voltage level states are characterised by either all high- or low-side switches conducting respectively. The figure highlights the transistor and diode in a conducting switch. In reality the current will flow through only one of the constituent solid-state devices. For instance, if the inverter is controlled in state 1 and the load current polarity is positive, then the IGBT is in conduction in the high-side switch of the load connected cell, and the diode is conducting in the low-side switch of the dc link connected cell.



a) State 0 **b) State 1**

c) State 2 **d) State 3**

Figure 2.3.7: Two-cell inverter limb operating states

The voltage level contribution of an *N*-cell inverter limb will depend on the number of high-side switches in conduction. Therefore, with *N* switches in conduction, the N^{th} voltage level is applied at the load terminal with respect to zero. This voltage can be expressed by

$$v_o = \frac{V_{dc}}{N}\sum_{n=1}^{N} S_n \qquad \ldots (2.3.1)$$

where the switch states are assigned S_0, S_1 … S_{N-1}, and logic '1' represents the high-side switch in conduction and the low-side switch in its inert state.

The total number of switching states in an *N*-cell inverter is given by 2^N. The number of states for the m^{th} voltage level, LEV_m, is the number of possible combinations of *m* logic '1's occurring in switching state *S*. These values lie in Pascal's (or Yanghui) triangle and can be calculated using the following formula

$$LEV_m = \frac{(N-1)!}{(N-1-m)!(m)!} \qquad \ldots (2.3.2)$$

The complexity of the inverter and the control task greatly increases with the number of cells. Table 2.3.1 shows the number of components and states in a flying-capacitor inverter as the number of cells is increased. The capacitor number is based on the assumption that the inverter is constructed using a unit capacitor size, and the dc link has *N* capacitors for an *N* cell inverter irrespective of phase number. In reality, the capacitor sizing will be based on the maximum link voltage, output load requirements and the practical implications of the semiconductor switch ratings and operating control scheme. Therefore, the table is purely an indication of inverter complexity

rather than a comparative reference. The row of data for a single cell inverter represents a conventional two-level case.

Cells	Single Phase Limb			Three-Phase Bridge		
	Load Voltage Levels	Switches	Capacitors	Load Voltage Levels	Switches	Capacitors
1	2	2	1	3	6	1
2	3	4	3	5	12	5
3	4	6	6	7	18	12
4	5	8	10	9	24	22
5	6	10	15	11	30	35
6	7	12	21	13	36	51

Table 2.3.1: Flying-capacitor inverter complexity

2.3.3 System Balancing Requirement

It has already been shown that there is more than one switching state capable of providing an intermediary level voltage at the load terminal of the inverter. If the cell-capacitors were ideal with infinite capacitance, then the control task would be relatively simple. However, in a real system the different switching states at a given voltage level lead to different current paths within the flying-capacitor inverter circuit. The current flowing through the cell-capacitors will cause the voltages to vary proportionally with the amplitude, duration and polarity of the current.

Increasing or decreasing capacitor voltage is related to the switch states in adjacent cells to the capacitor. If these switch states are not equal then current will flow in the capacitor. Figure 2.3.8 illustrates the two cases for current flow in a capacitor. As can be seen, if the upper switch state is ‘1’ and the lower ‘0’, then current will flow positively into the capacitor when the load current is positive and the capacitor voltage is increased. For the inverted switch state case, the voltage will decrease with a positive load current. The opposite is true for a negative load current. If the adjacent states are equal then the capacitor is bypassed and there is no effect on its voltage.

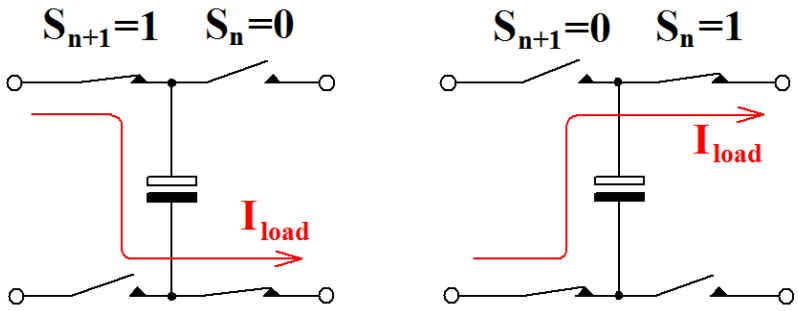


Figure 2.3.8: Current flow paths in a cell capacitor

In the case when there is a constant dc load current, then the inverter control will have to ensure that the time spent in each switching state is equal to achieve balanced capacitor operation. This will also ensure that the inverter is thermally balanced with the losses in the upper set of semiconductor switches are the same. The losses in the lower set of switches will also be the same, but not necessarily equal to the upper switches since the current direction is reversed, and so the diodes will conduct rather than the transistors. The amplitude of the voltage ripple in the cell-capacitor voltage will depend on the switching frequency chosen for control in respect to the capacitance and load current amplitude.

For an N-cell inverter when $m = 1$ or $m = N\text{-}1$, and the output voltage levels are V_{dc}/N or $(N\text{-}1)V_{dc}/N$ respectively, there are N different switching state possibilities (2.3.2). To affect the desired balanced operation, then the control must cycle through all N states when applying these two voltage levels. For inverters with $N > 3$, there are additional middle-range voltage levels with more than N different switching states. In the case when $N = 4$, there are 6 different switching states which give an output voltage of $V_{dc}/2$ with respect to the negative dc link. These are listed in Table 2.3.2. These states can be grouped into three complementary pairs: 3 & 12, 5 & 10 and 6 & 9. To accomplish the capacitor voltage and thermal balancing, it is only necessary to cycle through one of the switching state pairs. This is also the case for the half-voltage level in higher even cell number inverters.

State Number	Switching State S
3	0011
5	0101
6	0110
9	1001
10	1010
12	1100

Table 2.3.2: Switching states for 4-cell inverter, *m* = 2

When the cell number, *N*, is greater than 4 and is odd, then complementary pairing of states cannot be exploited for complete system balancing. Taking the 5 cell case as an example, there are 10 switching states for the mid-voltage levels listed in Table 2.3.3. In this case all 10 states must be cycled through to achieve balanced operation.

State Number	Switching State S
3	00011
5	00101
6	00110
9	01001
10	01010
12	01100
17	10001
18	10010
20	10100
24	11000

Table 2.3.3: Switching states for 5-cell inverter, *m* = 2

When the cell number is even, then the states between the half- and boundary voltage levels can be grouped through symmetry. For instance, the 6-cell inverter, at level m = 2 there are 15 different states, and 15 groups of three states can be identified which if cycled through will give balanced operation. The balancing sets for S in binary notation are listed as follows:

$$\left\{\begin{matrix}000011\\001100\\110000\end{matrix}\right\},\left\{\begin{matrix}000011\\010100\\101000\end{matrix}\right\},\left\{\begin{matrix}000011\\011000\\100100\end{matrix}\right\},\left\{\begin{matrix}000101\\001010\\110000\end{matrix}\right\},\left\{\begin{matrix}000101\\010010\\101000\end{matrix}\right\},$$

$$\left\{\begin{matrix}000101\\011000\\100010\end{matrix}\right\},\left\{\begin{matrix}000110\\001001\\110000\end{matrix}\right\},\left\{\begin{matrix}000110\\010001\\101000\end{matrix}\right\},\left\{\begin{matrix}000110\\011000\\100001\end{matrix}\right\},\left\{\begin{matrix}001001\\010010\\100100\end{matrix}\right\},$$

$$\left\{\begin{matrix}001001\\010100\\100010\end{matrix}\right\},\left\{\begin{matrix}001010\\010001\\100100\end{matrix}\right\},\left\{\begin{matrix}001010\\010100\\100001\end{matrix}\right\},\left\{\begin{matrix}001100\\010001\\100010\end{matrix}\right\},\left\{\begin{matrix}001100\\010010\\100001\end{matrix}\right\}$$

The numbers of states that constitute a balancing group at different voltage levels for a range of cell number inverters are listed in Table 2.3.4. These represent the minimum number of states which have to be cycled through in order to achieve balanced system control. The numbers in brackets are the total number of unique states at the given levels. Balancing of the inverter for low cell number inverters is relatively straightforward and can be accomplished by cycling through the small set of balancing states. These can be stored digitally in the control hardware keeping the complexity down to a minimum. Once the number of cells exceeds 6, then the large number of states which have to be incorporated within the control algorithm is excessive and so places huge demands on the control system.

Cell Number *N*	**Level Number *m***						
	1	**2**	**3**	**4**	**5**	**6**	**7**
2	2 (2)						
3	3 (3)	3 (3)					
4	4 (4)	2 (6)	4 (4)				
5	5 (5)	10 (10)	10 (10)	5 (5)			
6	6 (6)	3 (15)	2 (20)	2 (15)	6 (6)		
7	7 (7)	21 (21)	35 (35)	35 (35)	21 (21)	7 (7)	
8	8 (8)	4 (28)	56 (56)	2 (70)	56 (56)	4 (28)	8 (8)

Table 2.3.4: Minimum number of states for balancing

In the majority of multilevel inverter applications, the output voltage is a periodic waveform which approximates as closely as possible to a pure sinusoid. Therefore, the control can rotate through each member of the balancing set at a given voltage level

cycle by cycle. The premise being that in the steady-state, the current is equal at the same point in the cycle. Therefore, for low even cell number inverters, the number of cycles before a sequence of switching states is repeated is equal to the number of cells. In the case of a 5-cell inverter, this is twice the number of cells, because the half-voltage level requires all 10 states to be used. Figure 2.3.9 shows an example of this control method applied to a 3-cell inverter where the required sinusoidal output voltage is approximated by a staircase waveform. As can be seen, the switching states are different in each cycle at the same point in the output voltage waveform, and the cycling repeats after 3 cycles.

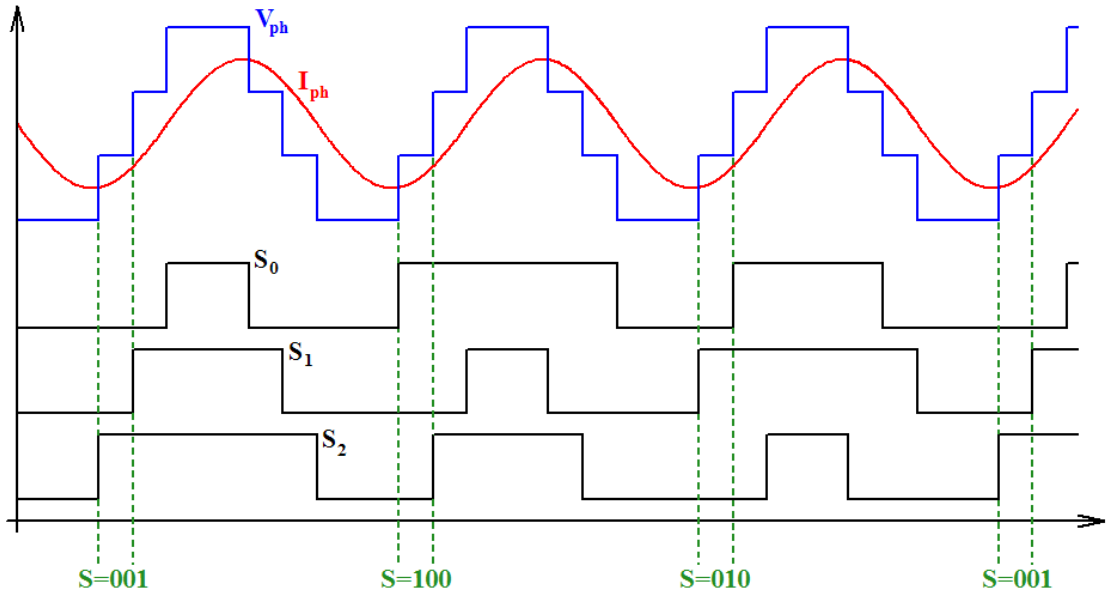


Figure 2.3.9: Firing waveforms for simple state rotation balancing in a three-cell inverter limb

In a real system, with finite voltage ripple on the cell-capacitors, this form of balancing will inevitably lead to sub- and inter-harmonic components being present in the output. With a repeating balancing pattern made up of a set of sequences of states every B cycles, then the lowest frequency component will be at f_1/B Hz where is f_1 is the target output fundamental frequency. These low frequency components are difficult to filter and can pose problems in a real load. Therefore, care must be taken in inverter capacitor selection in conjunction with control optimisation to minimise these effects.

There are a number of different sequence permutations, which will achieve the desired system balancing, and these increase with the number of inverter cells. The number of possible sequences, *SEQ*, is the product of the number of different states at each level.

In a cycle by cycle sequence rotation approach, then the number of possible patterns, P, is calculated by (2.3.4). These permutation numbers for a single phase limb are listed in Table 2.3.5.

$$P = \left(\frac{SEQ}{B} \right)^{x} \quad \ldots (2.3.4)$$

where

$$x = \sum_{n=1}^{B} n \quad \ldots (2.3.5)$$

Cell Number, *N*	**Number of Cycle Sequences, *SEQ***	**Minimum Cycle Number, *B***	**Number of Patterns, *P***
2	2	2	1
3	9	3	162
4	96	4	7962624
5	2500	10	3.460693×10^{30}
6	162000	6	2.789428×10^{29}
7	26471025	35	5.872562×10^{245}
8	1376829440	56	$3.504436 \times 10^{11795}$

Table 2.3.5: Number of balancing permutations

The excessive number of patterns for cell numbers greater than 4 makes pattern optimisation very difficult. By introducing rules to exclude certain sequences and combinations of sequences, then it may be possible to apply a pattern generation algorithm to the balancing control problem. For instance, switching frequency losses will be minimised by reducing the number commutation transitions within a sequence. Using only the sequences involving one switch state change per level transition will reduce the number of permutations. Alternatively, using cell-capacitor voltage feedback, the control itself can select the state or sequence within a cycle to maintain the capacitor voltages within the desired bands. The potential for ‘chaotic’ behaviour and the generation of unwanted very low frequency harmonics is clear especially in higher cell number inverters. These are the challenges faced in balancing the flying-capacitor inverter.

2.4 Modelling of Flying-Capacitor Inverter

2.4.1 Laplace Circuit Analysis of Capacitor Voltages

The two-cell flying-capacitor chopper circuit, shown in Figure 2.4.1, is the simplest form of the inverter topology family. There is only one capacitor and each power switch pair operate in a complementary manner so that there are four operating switching states.

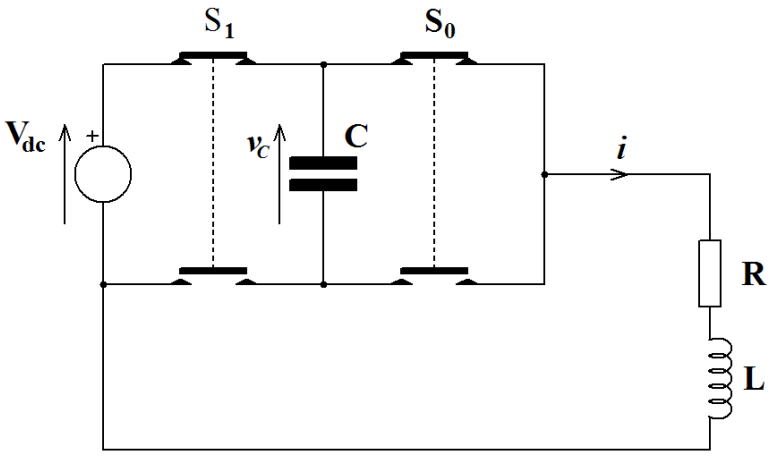


Figure 2.4.1: Two-cell inverter limb

The subject of this analysis, the capacitor voltage, is only connected in the circuit conduction path when the half voltage levels are applied across the load. The Laplace equivalent circuit for these two states [2.50], including the initial capacitor voltage v_{c0} and initial inductor current i_{L0}, are shown in Figures 2.4.2 and 2.4.3.

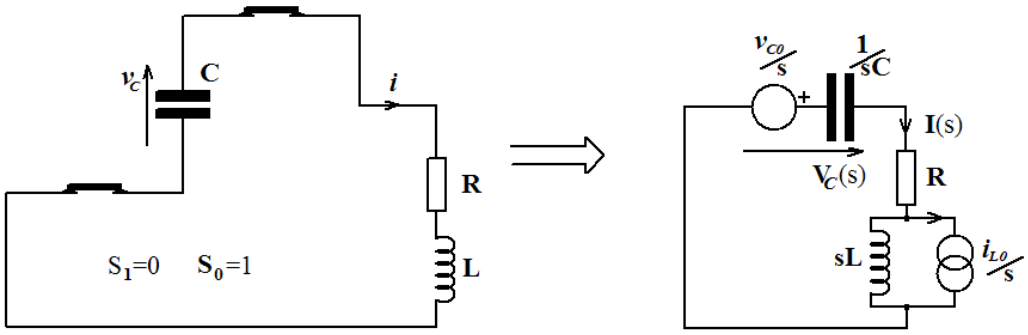


Figure 2.4.2: Laplace equivalent circuit for switch state 1

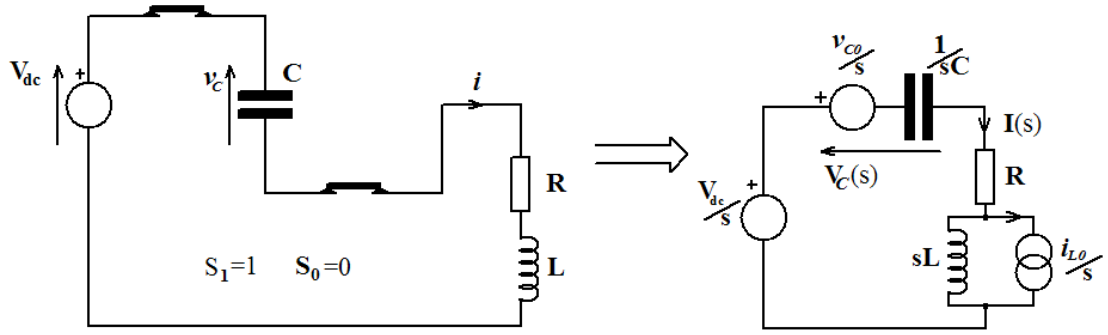


Figure 2.4.3: Laplace equivalent circuit for switch state 2

The Laplace transforms for state 1 are given by

$$V_C(s) = I(s)R + \left(sI(s)L - i_{L0}L\right) \quad \ldots (2.4.1)$$

$$I(s) = -C\left(sV_C(s) - v_{C0}\right) \quad \ldots (2.4.2)$$

By rearranging the equations (2.4.1 and 2.4.2), the state 1 Laplace transform for the capacitor voltage is given by

$$V_C(s) = \frac{v_{C0}CR + sv_{C0}CL}{\left(1 + sCR + s^2CL\right)} - \frac{i_{L0}L}{\left(1 + sCR + s^2CL\right)} \quad \ldots (2.4.3)$$

The Laplace transforms for state 2 are given by

$$V_C(s) = \frac{V_{DC}}{s} - I(s)R - \left(sI(s)L - i_{L0}L\right) \quad \ldots (2.4.4)$$

$$I(s) = C\left(sV_C(s) - v_{C0}\right) \quad \ldots (2.4.5)$$

By rearranging the equations (2.4.4 and 2.4.5), the state 2 Laplace transform for the capacitor voltage is given by

$$V_C(s) = \frac{V_{DC}}{s\left(1 + sCR + s^2CL\right)} + \frac{v_{C0}CR + sv_{C0}CL}{\left(1 + sCR + s^2CL\right)} + \frac{i_{L0}L}{\left(1 + sCR + s^2CL\right)} \quad \ldots (2.4.6)$$

In a high voltage system, the following relationship is true

$$v_{C0}CR >> i_{L0}L \quad \ldots (2.4.7)$$

In other words, the energy stored in the cell-capacitor is much larger than the energy stored in the load inductor. This means that the initial inductor current can be ignored. Therefore, the two switching state circuits can be combined into an equivalent circuit as shown in Figure 2.4.4. It has already been seen that for balanced operation, the time, T, in each state must be equal. Therefore, the input supply voltage is shown as a square-wave voltage with amplitude V_{dc}.

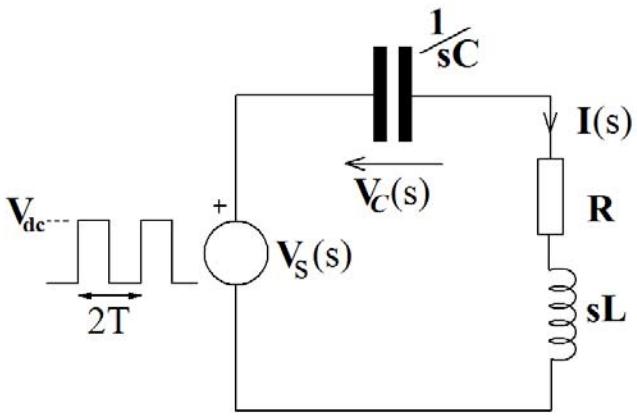


Figure 2.4.4: Two-cell inverter combined equivalent circuit

The Laplace transform of the capacitor voltage function is given by:

$$V_C(s) = \frac{1/sC}{\left(R + 1/sC + sL\right)} V_s(s) \quad \ldots (2.4.8)$$

where

$$V_s(s) = \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.9)$$

The final value of v_C can be found using the Final Value Theorem:

$$\lim_{t\to\infty} v_C(t) = \lim_{s\to 0} sV_C(s) \quad \ldots (2.4.10)$$

$$v_C(t \to \infty) = \frac{V_{dc}}{2} \quad \ldots (2.4.11)$$

Therefore, the two-cell flying-capacitor inverter will naturally balance with the average capacitor voltage at half the dc link, as long as the switching time for each of the two half-voltage states is equal. The capacitor is not in-circuit for the other two inverter states, and so the voltage will still reach the equilibrium voltage of half the dc link. It is also clear from the above analysis that if the times for the two half voltage states are not equal, then the mean capacitor voltage is a function of the ratio of state 1 period to the combined period of states 1 and 2. Therefore, the control must ensure averaged equal times for each state otherwise asymmetry will result in the output voltage. Any variation in the switching times will also be reflected in a similar variation in capacitor mean voltage, and potentially result in unwanted harmonics in the output.

The equivalent Laplace transform for the inverter can be used to find the time-domain equation for the system, and give some insight into capacitor voltage ripple and

charging transients. Equation (2.4.8) can be rewritten to incorporate a natural resonant frequency and damping factor for the 2nd order denominator term. This gives the following Laplace transform.

$$V_C(s) = \frac{\omega_n^2}{\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)} \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.12)$$

where

$$\omega_n = \sqrt{\frac{1}{CL}} \quad \ldots (2.4.13)$$

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \quad \ldots (2.4.14)$$

and the roots s_1 and s_2 are

$$s_1, s_2 = \zeta\omega_n \pm \omega_n\sqrt{\left(\zeta^2 - 1\right)} \quad \ldots (2.4.15)$$

$$\omega_n^2 = s_1 s_2 \quad \ldots (2.4.16)$$

To obtain the time-domain equation for the capacitor voltage, equation (2.4.12) is first factorised before performing the inverse Laplace transform [2.51].

$$V_C(s) = \frac{\omega_n^2}{(s + s_1)(s + s_2)} \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.17)$$

$$V_C(s) = \frac{A_1}{(s + s_1)\left(1 + e^{-Ts}\right)} + \frac{A_2}{(s + s_2)\left(1 + e^{-Ts}\right)} + \frac{A_3}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.18)$$

$$V_C(s) = \omega_n^2 V_{dc}\left[\begin{array}{l} \dfrac{1/s_1(s_1 - s_2)}{(s + s_1)\left(1 + e^{-Ts}\right)} + \dfrac{1/s_2(s_2 - s_1)}{(s + s_2)\left(1 + e^{-Ts}\right)} \\ + \dfrac{1/s_1 s_2}{s\left(1 + e^{-Ts}\right)} \end{array}\right] \quad \ldots (2.4.19)$$

The inverse Laplace transform of (2.4.19) will have the form shown below:

$$v_c(t) = \omega_n^2 V_{dc}\left(f_1(t) + f_2(t) + f_3(t)\right) \quad \ldots (2.4.20)$$

where

$$f_1(t) = \frac{1}{s_1(s_1 - s_2)} e^{-s_1 t}\left[\sum_{n=0}^{\infty} e^{nTs_1}(-1)^n u(t - nT)\right] \quad \ldots (2.4.21)$$

$$f_2(t) = \frac{1}{s_2(s_2 - s_1)} e^{-s_2 t}\left[\sum_{n=0}^{\infty} e^{nTs_2}(-1)^n u(t - nT)\right] \quad \ldots (2.4.22)$$

$$f_3(t) = \frac{1}{s_2 s_1}\left[\sum_{n=0}^{\infty}(-1)^n u(t-nT)\right] \quad \ldots (2.4.23)$$

Therefore, the time domain equation for the capacitor voltage is given by the following relationships, where *u(t)* is the unit step function,

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}\frac{\omega_n^2}{s_1 s_2}(-1)^n u(t-nT)\times \left(1+\frac{s_2}{(s_1-s_2)}e^{-s_1(t-nT)}+\frac{s_1}{(s_2-s_1)}e^{-s_2(t-nT)}\right) \quad \ldots (2.4.24)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}\frac{\omega_n^2}{s_1 s_2}(-1)^n u(t-nT)\times \left(1+\frac{\left(s_2 e^{-s_1(t-nT)}-s_1 e^{-s_2(t-nT)}\right)}{(s_1-s_2)}\right) \quad \ldots (2.4.25)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}(-1)^n u(t-nT)\times \left(1+\frac{e^{-\zeta\omega_n(t-nT)}}{2\omega_n\sqrt{\zeta^2-1}}\left(\begin{array}{l}\left(-\zeta\omega_n-\omega_n\sqrt{\zeta^2-1}\right)e^{\omega_n\sqrt{\zeta^2-1}(t-nT)}-\\ \left(-\zeta\omega_n+\omega_n\sqrt{\zeta^2-1}\right)e^{-\omega_n\sqrt{\zeta^2-1}(t-nT)}\end{array}\right)\right) \quad \ldots (2.4.26)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}(-1)^n u(t-nT)\times \left(1-\frac{e^{-\zeta\omega_n(t-nT)}}{\omega_n\sqrt{\zeta^2-1}}\left(\begin{array}{l}\zeta\omega_n\sinh\left(\omega_n\sqrt{\zeta^2-1}(t-nT)\right)+\\ \left(\omega_n\sqrt{\zeta^2-1}\right)\cosh\left(\omega_n\sqrt{\zeta^2-1}(t-nT)\right)\end{array}\right)\right) \quad \ldots (2.4.27)$$

The capacitor voltage waveform when the inverter is operated from a quiescent start has the form shown in Figure 2.4.5. This was plotted from equation (2.4.27) using MATLAB, with the circuit parameters C = 4.7 mF, R = 30 Ω, L = 100 mH, T = 50 ms and V_{dc} = 400 V. It can be seen that the mean capacitor voltage trajectory heads towards 200 V, the balanced target condition. The ripple voltage component of course can be reduced by switching at a higher frequency or increasing the capacitance.

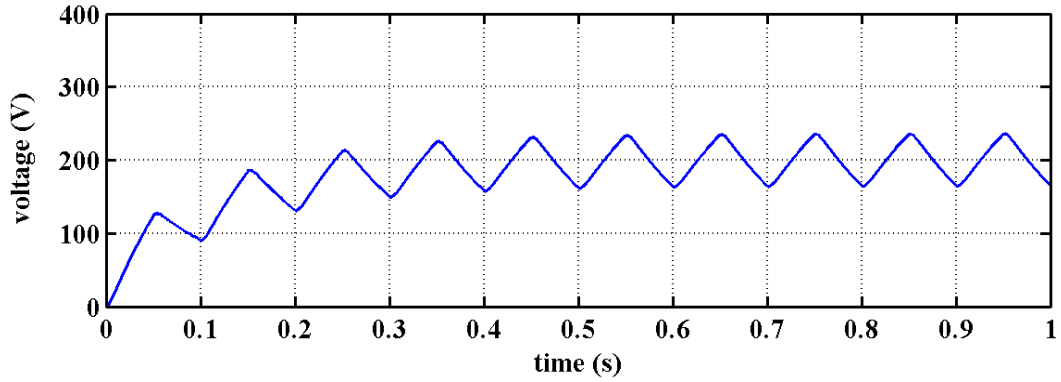


Figure 2.4.5: Transient build-up of the capacitor voltage

2.4.2 Laplace Analysis of Multi-Cell Circuit

The three-cell topology has two individual cell-capacitors and can operate with an additional intermediary voltage level. The number of switch modes is eight and each capacitor has four modes associated with its operation. Using the same analysis technique as in the two-cell case, the Laplace transform for each cell capacitor voltage can be derived. As before in the analysis, the cases when a capacitor is not in circuit with the load are ignored.

Taking the case of the three states, with only one upper switch on in each cell, and giving the lowest intermediary output voltage. This results in two simultaneous equations for each capacitor.

$$V_{C_0}(s) = \frac{\omega_n^2}{(s+s_1)(s+s_2)} \frac{V_{C_1}(s)}{s\left(1+e^{-Ts}\right)} \quad \ldots (2.4.28)$$

$$V_{C_1}(s) = \frac{\omega_n^2}{(s+s_1)(s+s_2)} \left(\frac{V_{dc}}{s\left(1+e^{-Ts}\right)} - \frac{e^{-Ts} V_{C_0}(s)}{s\left(1+e^{-Ts}\right)} \right) \quad \ldots (2.4.29)$$

Using Final Value Theorem (2.4.9):

$$sV_{C_0}(s)|_{s=0} = \frac{sV_{C_1}(s)|_{s=0}}{2} \quad \ldots (2.4.30)$$

$$sV_{C_1}(s)|_{s=0} = \frac{V_{dc} - sV_{C_0}(s)|_{s=0}}{2} \quad \ldots (2.4.31)$$

$$v_{C_0}(t \to \infty) = \frac{V_{dc}}{3} \quad \ldots (2.4.32)$$

$$v_{C_1}(t \to \infty) = \frac{2V_{dc}}{3} \quad \ldots (2.4.33)$$

The same analysis method used for the second level voltage modes, when two switches are on, also reveals the same result. This analysis in part has proven the natural voltage balancing of the flying-capacitor inverter circuit when all modes with equal voltage levels are used with equal time duration. The analysis can be further extended to higher cell numbers, resulting in the following set of simultaneous equations.

$$V_{C_0}(s) = \frac{\omega_n^2 V_{C_1}(s)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.34)$$

$$V_{C_1}(s) = \frac{\omega_n^2 \left(V_{C_1}(s) - e^{-Ts} V_{C_0}(s)\right)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.35)$$

$$V_{C_{N-1}}(s) = \frac{\omega_n^2 \left(V_{dc} - e^{-Ts} V_{C_{N-2}}(s)\right)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.36)$$

Once the levels increase above 2-cells it is very difficult to derive a usable standard time-domain equation for the cell-capacitor voltages since it is dependent on the sequence of switching states and any pattern thereof. Therefore, for higher cell numbers an approach other than Laplace circuit analysis is required for modelling in order to simulate the different waveforms in the system.

2.4.3 Simple Circuit Model of Converter

The fundamental operation and characteristics of the flying-capacitor converter has been shown to offer a great deal of flexibility in terms of operating modes compared to conventional two-level bridges. Complexity increases dramatically as the number of levels increases and this makes it difficult to analyse operation without resorting to computer-aided circuit simulation. Therefore, a simple mathematical model is developed which can be used in MATLAB to simulate the ideal system waveforms under different control schemes.

The state-space equations for the inverter are used to construct a set of matrix equations linking the cell-capacitor voltages and the output load voltage and current. It is preferable that the equations are in a generalised form applicable to any N-cell inverter and that the power switch states vector is included separately. The following set of matrix equations was derived for the generalised N-cell inverter limb shown in Figure 2.4.6.

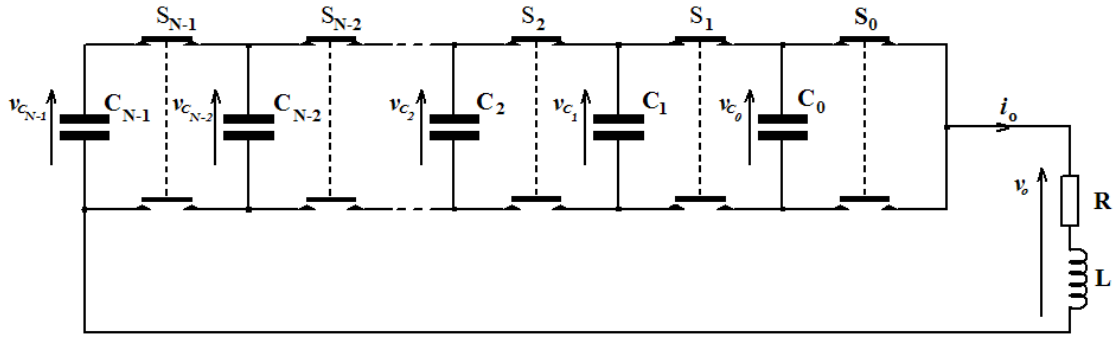


Figure 2.4.6: N-level flying-capacitor inverter limb

The three matrix based equations governing the system on a simple RL load are

$$\frac{\mathbf{dV_C}}{\mathbf{dt}} = -\mathbf{C}\mathbf{J}^{\mathbf{T}}\mathbf{S}i_o \qquad \ldots (2.4.37)$$

$$v_o = \left(\mathbf{S}^{\mathbf{T}}\mathbf{J}\right)\mathbf{V_C} \qquad \ldots (2.4.38)$$

$$\frac{di_o}{dt} = \frac{1}{L}\left(v_o - R.i_o\right) \qquad \ldots (2.4.39)$$

where

$$\mathbf{V_C} = \begin{bmatrix} v_{C_{N-1}} \\ v_{C_{N-2}} \\ \ldots \\ v_{C_2} \\ v_{C_1} \\ v_{C_0} \end{bmatrix}, \ \mathbf{S} = \begin{bmatrix} S_{N-1} \\ S_{N-2} \\ \ldots \\ S_2 \\ S_1 \\ S_0 \end{bmatrix}, \ \mathbf{J} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & \ldots \\ 0 & 1 & -1 & 0 & \ldots & 0 \\ \ldots. & \ldots & \ldots. & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 1 & -1 & 0 \\ 0 & \ldots & 0 & 0 & 1 & -1 \\ \ldots & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1/C_{N-1} & 0 & 0 & 0 & 0 & \ldots \\ 0 & 1/C_{N-2} & 0 & 0 & \ldots & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 1/C_2 & 0 & 0 \\ 0 & \ldots & 0 & 0 & 1/C_1 & 0 \\ \ldots & 0 & 0 & 0 & 0 & 1/C_0 \end{bmatrix}$$

By convention $v_{C_{N-1}} = V_{dc}$ in the is the cell-capacitor voltage vector, $\mathbf{V_C}$.

The relationships contain a form of Jordan matrix, **J**, which links the switching states and the cell capacitor voltages to the phase output voltage. These matrix relationships governing the flying-capacitor inverter circuit can be incorporated within a simple

fixed time-stepping procedure to obtain the load voltage v_o and current i_o variation with a particular switch state operated over a time period. By combining different switch states operated over different time-periods any switching sequence pattern can be simulated rapidly.

For example, a MATLAB script was run to simulate one two-cell inverter limb operating in a half-bridge configuration, where one end of the load is tied to $V_{dc}/2$. Figure 2.4.7 shows the resultant load voltage and current waveforms in the steady-state condition when the inverter is operated with a simple 50 Hz staircase control scheme. The circuit parameters for this simulation were V_{dc} = 400 V, R = 10 Ω, L = 30 mH and C = 1 mF. It can be seen from the load voltage waveform that the capacitor voltage variation affects the zero voltage level, and interestingly may 'improve' the shape of the waveform, and reduce some of the unwanted harmonic components if the control and capacitance are optimised correctly. This feature has been explored in the full-bridge configuration using this matrix-based modelling as a tool and the results presented at the EPE conference, 2001 [2.52].

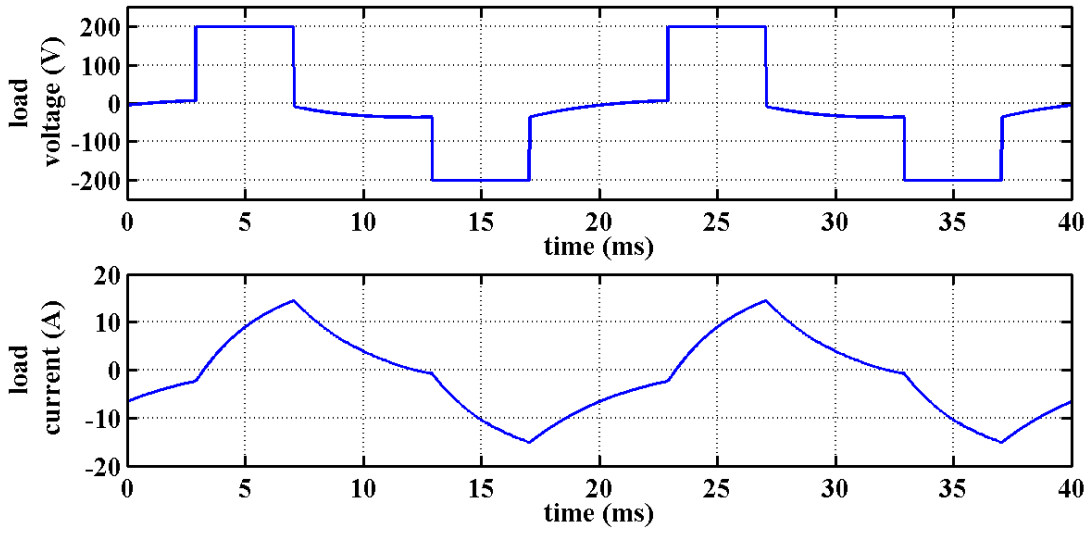


Figure 2.4.7: Two-cycles of steady-state load waveforms

The trajectory of the capacitor voltage increase from a quiescent start can be seen in Figure 2.4.8. It shows that the capacitor voltage will self-balance to $V_{dc}/2$ as expected with the half-voltage states swapping control between each cycle.

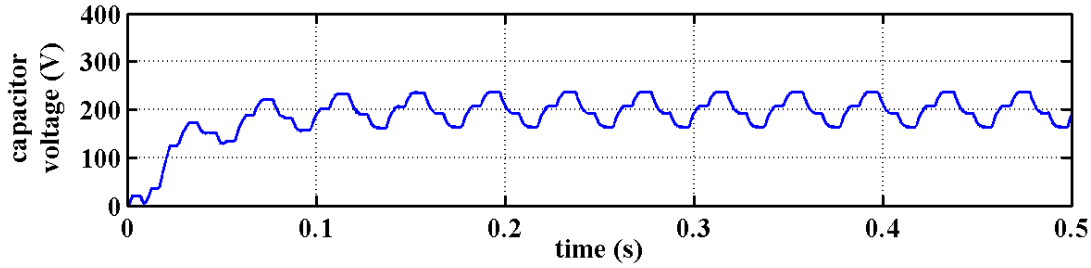


Figure 2.4.8: Capacitor voltage build-up from inert state

2.5 Development of an Inverter Simulator

2.5.1 Simulator Software Design

There are various software tools and simulation packages available for investigating power electronic converters and drives. In the past, computer aided design (CAD) packages have been developed by researchers investigating PWM connected power electronic systems. Bowes et al. at Bristol developed their own CAD package, BTRAP, to aid their PWM research [2.53]. Gateau et al. at Toulouse, however, adopted commercial packages, using a combination of SABER for power electronics and ModelSim for control logic VHDL for simulating the flying-capacitor inverter system [2.54].

Only one such simulation package was available during the project, SIMULINK, a graphical simulation addition to MATLAB. Some investigations were undertaken using the Power System Block Set, a SIMULINK toolbox containing power device and other circuit block models relevant to power electronics systems. However, it was found that the simulation time for one sinusoidal cycle was around 5 minutes on a reasonably fast computer which make very detailed simulation over a sufficient period very time consuming. Since the block set is a proprietary product, full analysis of operating parameters such as switching loss is difficult. Therefore, it was felt that a bespoke solution was needed for this project, allowing full control over the inherent sub-system modelling and offering significantly increased simulation speeds.

The development platform chosen for this work is Microsoft Visual C++, making use of the graphical user interface capabilities in Windows and the power of the C++ programming language [2.55]. A set of library classes implement various circuit elements, using object oriented programming (OOP) techniques to allow fast development of more complex system models [2.56].

In the real world any object can be thought of as having characteristics, or states, and behaviour. OOP uses this principle to instantiate (create) objects within the software,

whereby each object has variables (states) and functions or methods (behaviour). In C++, the class is the blueprint for an object and contains the necessary code to define the required object. This approach helps with modularity in terms of maintaining software, and any modifications can take place at the class level. Different objects which share common traits can be instantiated through the use of derived subclasses. This is achieved by defining an abstract class with generic states and behaviour and then through inheritance defining subclasses which have modifications for the actual objects required. This allows efficient software reuse and behaviour enhancements to be done at the abstract class level.

Applying these OOP techniques to the problem in hand, the base class for circuit simulation is an abstract class which models a two-terminal electrical component with associated behaviour common to all electrical components, i.e. a voltage appears at its terminals when a current flows through it. Derived classes can then include the standard linear components: resistor, capacitor and inductor. A specific method for obtaining the voltage or current at a specific instance in time is used in each case. This uses the basic piecewise linear circuit equations for the component for a small fixed time-step. Using these classes, more complex circuits can be modelled by instantiating each component in the code. Some degree of knowledge has to be adopted, since stable simulations are more likely to be achieved if the integral circuit equations are used for obtaining nodal voltages or currents for passive energy storage devices. Figure 2.5.1 illustrates the simplified class hierarchy of the modelling C++ library.

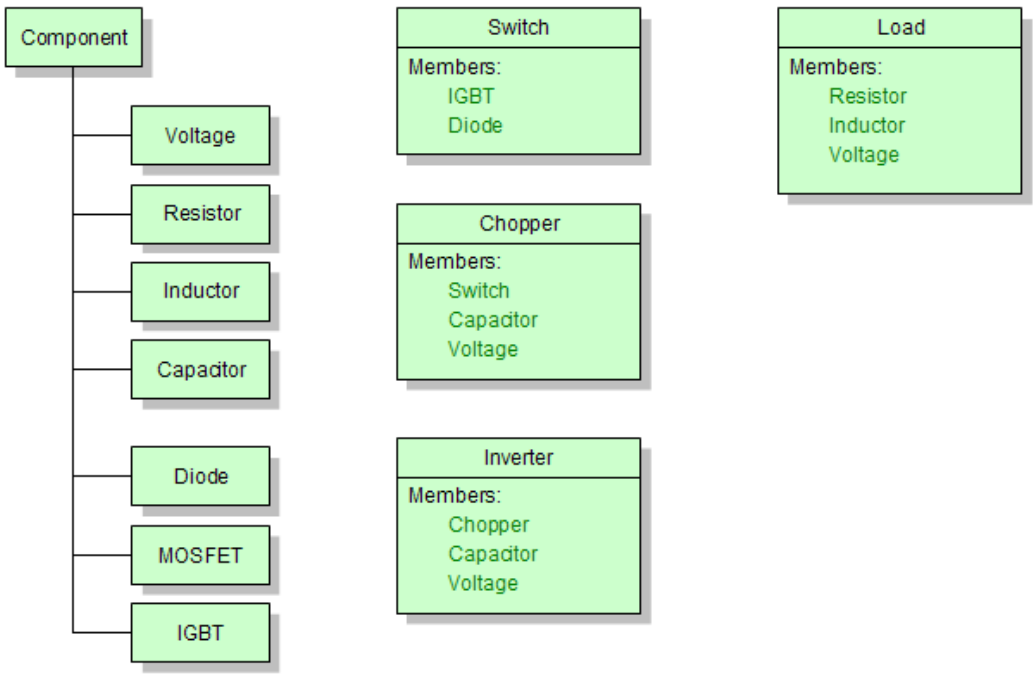


Figure 2.5.1: Class hierarchy and derived simulation classes

Taking these modelling concepts a stage further, nonlinear devices can be added by creating additional classes. In the case of electronic devices, and specifically power switching devices, the voltage characteristic when the device is conducting typically exhibits a nonlinear characteristic. For a simple class model, the device class could incorporate resistor and voltage classes as member variables. Alternatively, the V-I characteristic can be modelled using a look-up table of manufacturers published characteristics. This is the preferred method used in the simulator, and allows for the nonlinear behaviour with temperature to be included. Additionally, electronic device classes include methods for storing the energy absorbed in the device during a switching transition, and this can be done by either using tables of the manufacturer's published data where available or computing the curves using standard formulas for the turn-on or turn-off energy characteristics [2.57].

The complete power converter circuit is modelled as a combination of passive components and nonlinear solid-state switches. Each limb of the flying-capacitor inverter is instantiated using a Chopper class which contains the required number of inverter cells. The complete inverter class is then made up of three Chopper classes. The switching behaviour is controlled via time-stepping code which mimics the digital controller functionality. The different control modulator implementations have been modelled as C++ classes to mimic as closely as possible the likely implementation in a field programmable gate array (FPGA). Gate drive signals control the behaviour of the electronic switch models which in turn control the application of voltage to the load model. When the simulation is run, vectors of computed data are stored for visual display and post-processing.

A graphical user interface (GUI) has been developed using Microsoft Visual C++ development environment, which provides various controls and input data fields in order to improve the usability of the underlying simulator. A screen shot of the complete simulator is shown in Figure 2.5.2. As can be seen, the user interface dialog screen has various controls and edit boxes for selecting and setting the operating control parameters, inverter components and load characteristics. There is an oscilloscope style display for the load operating waveforms, a spectrum analyser display and a text box for displaying the key simulated operating conditions. The spectral components for the load voltage and current waveforms are found using a fast Fourier transform (FFT) written in C++ for the simulator.

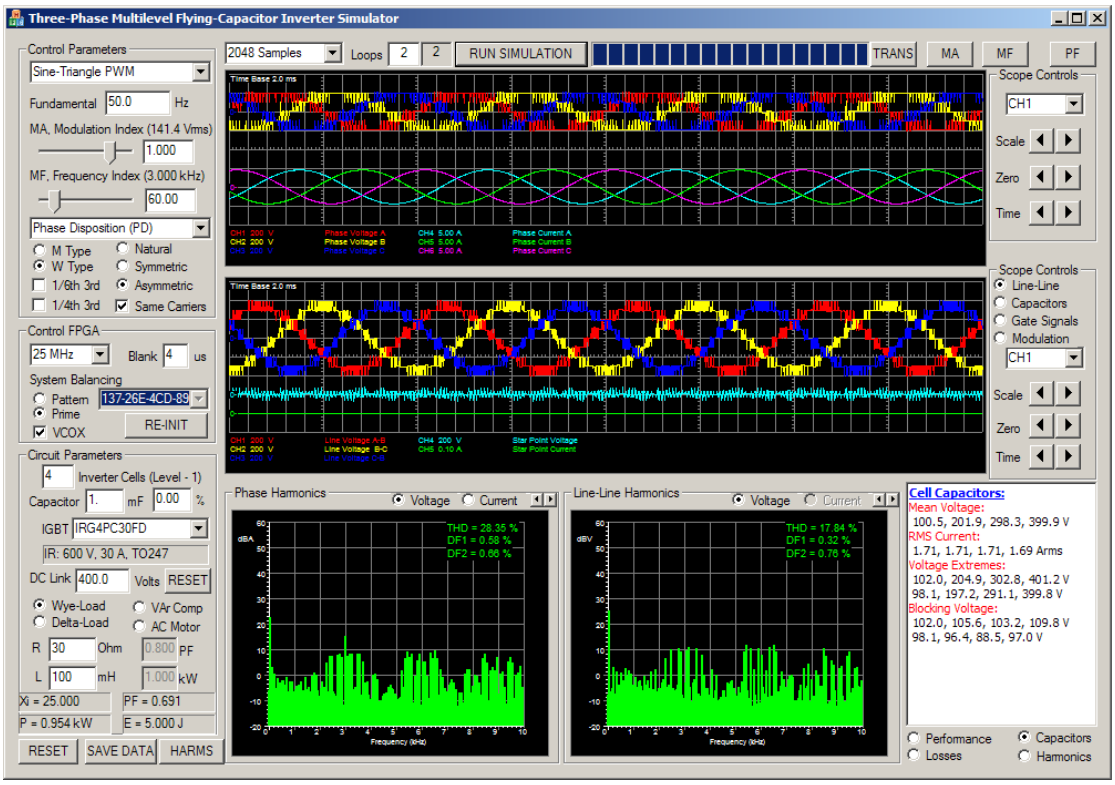


Figure 2.5.2: Simulator graphical user interface

2.5.2 Computation of Harmonic Distortion

The standard figure of merit regarding harmonic content in a waveform is the total harmonic distortion (THD) which expresses as a ratio the amount of unwanted harmonic content to the fundamental, V_1 [2.58]. The standard formula is

$$THD = \frac{100}{V_1}\sqrt{\sum_{n\neq 1} V_n^2} \quad \% \qquad \ldots (2.5.1)$$

A further two terms have been adopted in the literature specifically for quantifying PWM inverter output power quality [2.59, 2.60]. They are distortion factor 1 (DF1) and distortion factor 2 (DF2) and are computed from the following equations,

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n}\right)^2} \quad \% \qquad \ldots (2.5.2)$$

$$DF2 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n^2}\right)^2} \quad \% \qquad \ldots (2.5.3)$$

DF1 is applicable to ac motor drives which exhibit first order attenuation and it has also been referred to as the weighted THD (WTHD) [2.61]. The DF2 term is applicable to ac systems which have a second order L-C filter between the output of the inverter and the load.

The comparative assessment of sinusoidal modulation schemes is normally based on these THD and DF1 figures of merit and computed by the fast Fourier transform algorithm (FFT) from the voltage and current waveforms. Ideally the flying-capacitor inverter is operated with balanced cell-capacitor voltages at the ideal voltage levels with equal-spacing between the levels. In reality, without infinite capacitance, this will not be the case. There will be errors in the mean voltages and the voltages themselves will have ripple. This will inevitably lead to further harmonic distortion in inverter voltages.

It has been shown that the balancing of a multilevel inverter can lead to the generation of significant sub- and inter-harmonic frequency components at multiples of the fundamental divided by the number inverter cells per phase. It is already a known phenomenon in standard inverters and some researchers take this into account [2.62]. To ensure that these components are not ignored, the THD and DF1 equations need to be modified to take into account the number of levels in a multilevel inverter. The assumption is that any FFT algorithm is applied to data captured in a time window encompassing *m* multiples of the fundamental period, where *m* is the number of cells in the flying-capacitor inverter. The following equations are the modified forms of the classic distortion factors used in the literature.

$$THD = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} V_{i/m}^2 - V_1^2} \ \% \qquad \ldots (2.5.4)$$

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} \frac{m^2 V_{i/m}^2}{i^2} - V_1^2} \ \% \qquad \ldots (2.5.5)$$

These issues are important in understanding harmonic distortion, especially in the case of multilevel inverters. The literature is full of comparisons based on these analytical expressions, and there is a danger that the true nature of harmonic distortion is overlooked. The real definition of THD is shown in equation (2.5.6), where it is a true measure of the unwanted harmonic component in the output power.

$$THD = \frac{100}{\tilde{V}_1}\sqrt{\tilde{V}_T^2 - \tilde{V}_1^2} \ \% \qquad \ldots (2.5.6)$$

where

$\tilde{V}_1$ is the fundamental rms voltage

$\tilde{V}_T$ is the total rms voltage

The simulator also computes the THD of the output voltage and current using the rms value and the fundamental amplitude from (2.5.6). The figures obtained, if computed from simulated data over a long time-frame, will include any multi-cycle repeating

very low frequency harmonic components which may be present due to the control scheme used.

2.5.3 Cell-Capacitor Requirement Indicator

The value and rating of the required cell-capacitors in the flying-capacitor inverter has the most important bearing on overall system size and cost. Firstly, the capacitors must be rated to handle the rms ripple current seen during normal operation. Secondly, the capacitance must be sufficiently high to ensure that the cell-voltages do not deviate too greatly from their balanced values, causing over-voltage conditions on the semiconductor switches.

The simulator provides current data for each capacitor which can be used for capacitor selection. Capacitor manufacturers provide lifetime figures for different ambient temperatures, operating frequencies and ripple currents, so that the inverter can be designed to meet the minimum required lifetime expectancy.

The minimum capacitance required is dependent on the cell-capacitor current amplitude as a function of time. The voltage variation is a function of the integral of current during a switching state and the net contribution due to the balancing control method used. Therefore, for a given synthesised fundamental frequency, higher capacitance is needed for lower inverter switching frequencies, with staircase SHE control being the worst case, To aid in characterising the inverter's performance at a specific synthesising frequency for different balancing and control schemes and load characteristics, it is helpful to use a system parameter which relates the unit cell-capacitor stored energy to the total load power of the three-phase inverter. It is especially instructive when analysing the characteristics of the inverter when operating under staircase SHE control.

The system parameter used throughout the analysis is termed the energy factor, ξ, and can be used for comparative analysis of different control schemes and operating parameters. The energy factor mathematical derivation is as follows:

The basic load real power is given by

$$P = \tilde{I}_a^2 R_a + \tilde{I}_b^2 R_b + \tilde{I}_c^2 R_c \qquad \ldots (2.5.7)$$

and assuming the load is balanced

$$P = 3\tilde{I}_{ph}^2 R \qquad \ldots (2.5.8)$$

The phase current rms $\tilde{I}_{ph}$ can be replaced with the phase voltage rms. $\tilde{V}_{ph}$. and power factor of the fundamental $\cos\phi$ to give

$$P = \frac{3\left(\tilde{V}_{ph}\cos\phi\right)^2}{R} \quad \ldots (2.5.9)$$

Now the phase voltage rms is a function of the dc link voltage, V_{dc} and amplitude modulation index, m_a, so (2.5.9) can be rearranged to give

$$P = \frac{3}{R}\left(\frac{m_a V_{dc}}{2\sqrt{2}}\cos\phi\right)^2 \quad \ldots (2.5.10)$$

In an N-cell inverter, the unit cell-capacitor voltage is

$$V_c = \frac{V_{dc}}{N} \quad \ldots (2.5.11)$$

so rearranging (2.5.10) gives

$$P = \frac{3}{R}\left(\frac{m_a N V_c}{2\sqrt{2}}\cos\phi\right)^2 \quad \ldots (2.5.12)$$

Equation (2.5.12) can be rearranged to separate the unit cell-capacitor energy to give

$$P = 3\left(\frac{\left(m_a N\cos\phi\right)^2}{4RC}\right)\left(\frac{1}{2}CV_c^2\right) \quad \ldots (2.5.13)$$

and where the unit cell-capacitor stored energy, E_c, is given by

$$E_c = \frac{1}{2}CV_c^2 \quad \ldots (2.5.14)$$

Simplifying results in the following relationship

$$P = \xi N^2 m_a^2 \cos^2\phi E_c \quad \ldots (2.5.15)$$

where

$$\xi = \frac{3}{4RC}\ \text{s}^{-1} \quad \ldots (2.5.16)$$

In a practical system, the designer would aim to minimise the capacitor size which can lead to increased voltage ripple on the capacitors. So the parameter, ξ, needs to be as large as realistically possible, while maintaining safe operation of the inverter by minimising the peak switch blocking voltages and peak capacitor voltages. The ripple voltage will also be dependent on the amount of current flowing when the capacitors are in the load current path. Therefore, the current lag angle, ϕ, is also an instructive parameter when quantifying the inverter performance with the system design parameters. It is simply related to the load parameters thus,

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) \quad \ldots (2.5.17)$$

The term, $cos\phi$, is the power factor for an ideal sinusoidal system. It is usually referred to as displacement factor (DPF) to differentiate it from the true power factor (TPF), which is defined as the ratio of real power to apparent power. The displacement power factor of the load is the preferred parameter for analysis of the system and is used throughout the simulations to allow inverter performance comparisons, independent of the power rating and input voltage of the system.

2.5.4 Generic Load Model

The cell-capacitor voltage variation depends on the amplitude and polarity of the load current at intermediary output voltage levels when the capacitor is in circuit. Therefore, the position of the peak of the ideal sinusoidal current with respect to these intermediary voltage levels will affect performance. The angle, ϕ, between the phase current with the phase voltage is dependent on the load characteristics. Therefore, the displacement power factor term, $cos\phi$, is important in quantifying the load characteristic and for comparing the performance of different modulation strategies in the flying-capacitor circuit.

In the case of inductive loads, where the current lags the voltage, the inductance and resistance also dictate the effective filtering of the voltage harmonics seen in the phase current. Rather than limiting load modelling as a simple RL, a more generic approach is adopted by the addition of an idealised e.m.f. sinusoidal voltage term. This gives a good approximation to a load applicable to most ac systems, and has been adopted by other researchers in the past [2.63]. More complex load models could have been adopted, but since of the investigation is focussed specifically on the inverter and the cell-capacitor voltages, and the current distortion is relatively low, then this generic load model is appropriate. Figure 2.5.3 shows the circuit of a star-connected generic load used in the simulator.

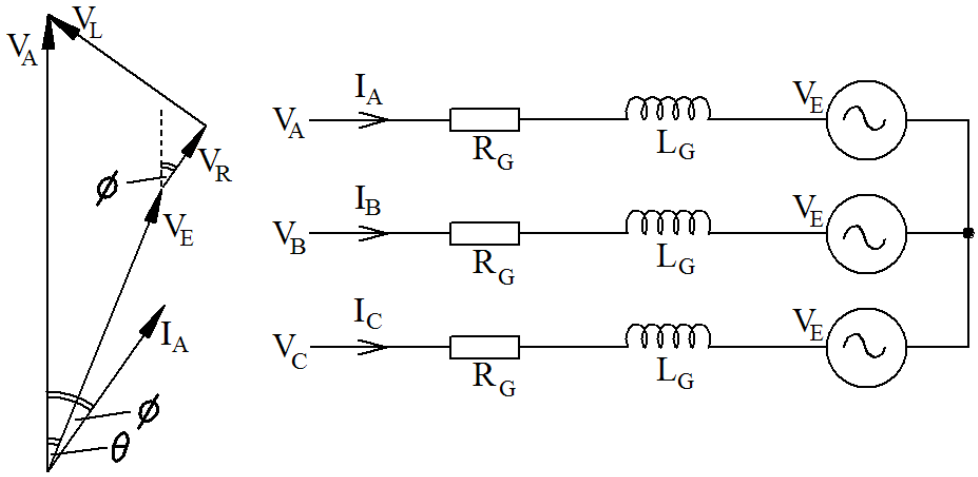


Figure 2.5.3: Generic load model circuit and voltage phasor diagram

The voltage relationships between the load and the phase voltage are given by

$$V_E \sin\theta = V_L \cos\phi - V_R \sin\phi \qquad \ldots (2.5.18)$$

$$V_E \cos\theta = V_A - V_L \sin\phi - V_R \cos\phi \qquad \ldots (2.5.19)$$

where

V_L and V_R are the voltages across R_G and L_G respectively.

There is only one unique solution of R_G and L_G value at the given fundamental frequency for the case when the e.m.f. term is zero and these are R and L in the RL load case. When the back e.m.f. is finite, then there is a range of values of R_G, L_G, V_E and θ which can be used to match the lag angle in the current and output load power. Therefore, when modelling the load system, the resistance, inductance, real power P and displacement power factor $\cos\phi$ are specified. For instance, if the load aims to model an induction motor, then the R_G parameter is the stator winding resistance and the L_G parameter is the leakage inductance. The simulator then computes the required e.m.f. term amplitude V_E and phase shift θ in the following manner.

$$I_{ph} = \frac{P}{3V_{ph}\cos\phi} \qquad \ldots (2.5.20)$$

$$V_R = I_{ph} R_G \qquad \ldots (2.5.21)$$

$$V_L = 2\pi f L_G I_{ph} \qquad \ldots (2.5.22)$$

$$\theta = \tan^{-1}\left(\frac{V_L \cos\phi - V_R \sin\phi}{V_A - V_L \sin\phi - V_R \cos\phi}\right) \qquad \ldots (2.5.23)$$

$$V_E = \frac{V_L \cos\phi - V_R \sin\phi}{\sin\theta} \qquad \ldots (2.5.24)$$

It has already been seen that significant voltage ripple on the flying-capacitor inverter capacitors will lead to significant low order harmonic content in the output phase voltage. Therefore, the resultant current THD will be more representative when using a non-zero e.m.f. parameter in the load model, compared with the basic RL case.

Finally, the equivalent energy factor, ξ, cannot be calculated directly using (2.5.16) as in the simple RL load case. For generic load simulation where the desired output power, P, and the DPF, $cos\phi$, are set, then ξ can be calculated using the following derivation

$$P = \frac{3\left(\tilde{V}_{ph}\cos\phi\right)^2}{R} \qquad \ldots (2.5.25)$$

where

R is the equivalent resistance for an RL load

The phase voltage rms in terms of the dc link voltage and amplitude modulation index is given by

$$\tilde{V}_{ph} = \frac{m_a V_{dc}}{2\sqrt{2}} \qquad \ldots (2.5.26)$$

so rearranging (2.5.25) to obtain a relationship for R gives

$$R = \frac{3\left(m_a V_{dc}\cos\phi\right)^2}{8P} \qquad \ldots (2.5.27)$$

This can now be used in conjunction with the original energy factor equation (2.5.16) to give a modified equation for computing ξ in the simulator,

$$\xi = \frac{2P}{CV_{dc}^2 m_a^2 \cos^2\phi} \qquad \ldots (2.5.28)$$

2.6 Conclusions

The flying-capacitor inverter is an interesting member of the multilevel inverter family, but it has been the least popular for development in new application, and has had fewer research studies dedicated to its operation. This is primarily due to the number of required cell-capacitors which are crucial to its operation and impact significantly on the inverter's size, cost and performance. It is clear, therefore, that optimising the control must focus on reducing capacitor rating while achieving the lowest possible harmonic distortion in the load waveform without compromising safe-operation and the life-time of the power electronic switches.

It has been shown that the increasing level of complexity in terms of the number of operating states, especially as more inverter cells are added, provides a great challenge on the analysis and design of the control system. Nevertheless, as has been shown, the system balancing requirements can be met by correct switching state rotation.

There are many multilevel control schemes which can be applied to a three-phase flying-capacitor inverter, and they all offer different merits in terms of output harmonic signature and operating switching frequencies in the ideal case. When practical sized capacitors are used in the system, then the influence of voltage ripple needs a more detailed examination when operating with the different control schemes.

It has been shown that some operating information can be obtained using basic circuit analysis and modelling techniques. However, the need for rapid and more detailed modelling of the inverter system justified the development of a bespoke simulator package, which will aid the investigation of control approaches, and the effect of capacitor voltage ripple on performance.

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