Modelling and Control of a Flying-Capacitor Inverter

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Abstract:

This paper presents the results of an investigation into the variation in the output voltage quality of a flying-capacitor inverter under staircase angle control. The trade-offs between capacitor size, power device voltage rating and output voltage quality are assessed through simulation. A general mathematical model for an N-level inverter is used for circuit operation analysis and its results are compared with those from a Simulink® circuit simulation. The computer model allows a thorough investigation of all possible switching pattern permutations that produce the desired sinusoidal output and maintain steady state capacitor voltage balancing. Results show that the total harmonic distortion in a sinusoidal synthesised output can be minimised by the correct selection of the switching mode sequence.

Keywords:

multilevel converters, modelling, power quality, harmonics

Introduction

Multilevel inverters are a class of power switching topologies aimed at high power applications such as motor drives and static power conditioning systems. A conventional full-bridge inverter can apply only two levels of voltage other than zero across their load. In multilevel inverters, an increased number of power switches are configured to provide several levels of voltage to the load. The inverter can then be controlled to synthesise an approximate sinusoid from the voltage levels available. Multilevel inverters have several benefits compared with the standard full-bridge inverter. They allow existing power switches to be used in systems where the dc-link and output voltages are higher than the individual switch ratings, and the individual power device operating frequency can be reduced through the increased voltage synthesis flexibility offered by the extra voltage levels. In motor drives, the voltage stress across the winding is reduced due to the lower voltage steps applied.

There are three main multilevel inverter topologies [1]:

- cascaded-cell
- diode-clamped
- flying-capacitor

The earliest examples of multilevel inverters described in the literature are now known as cascaded-cell forms. For example, McMurray's power converter for a sonar transducer [2] patented in the late 1960s. The next inverter form to appear was the neutral-point-clamped (diode-clamped), first patented in the 1970s by Baker [3]. Commercial products using both types are now available, mainly for high voltage, high power, induction motor drives.

The flying-capacitor or imbricated-cell multilevel inverter is a more recent alternative topology where capacitors are used directly to clamp the voltages of the power switch chain nodes. The three-cell implementation of this circuit is shown in Figure 1. Present interest in the circuit stems from the work of Meynard and Foch [4, 5] in the early 1990s. The basic principle of operation is similar to the switched capacitor chopper described in the early 1970s by Singer et al. [6]. The power switches are

operated as complementary pairs (S_{L1} and S_{L1}', etc.), and intermediary voltage levels are realised by routing the load current through paths that include the clamping- or cell-capacitors.

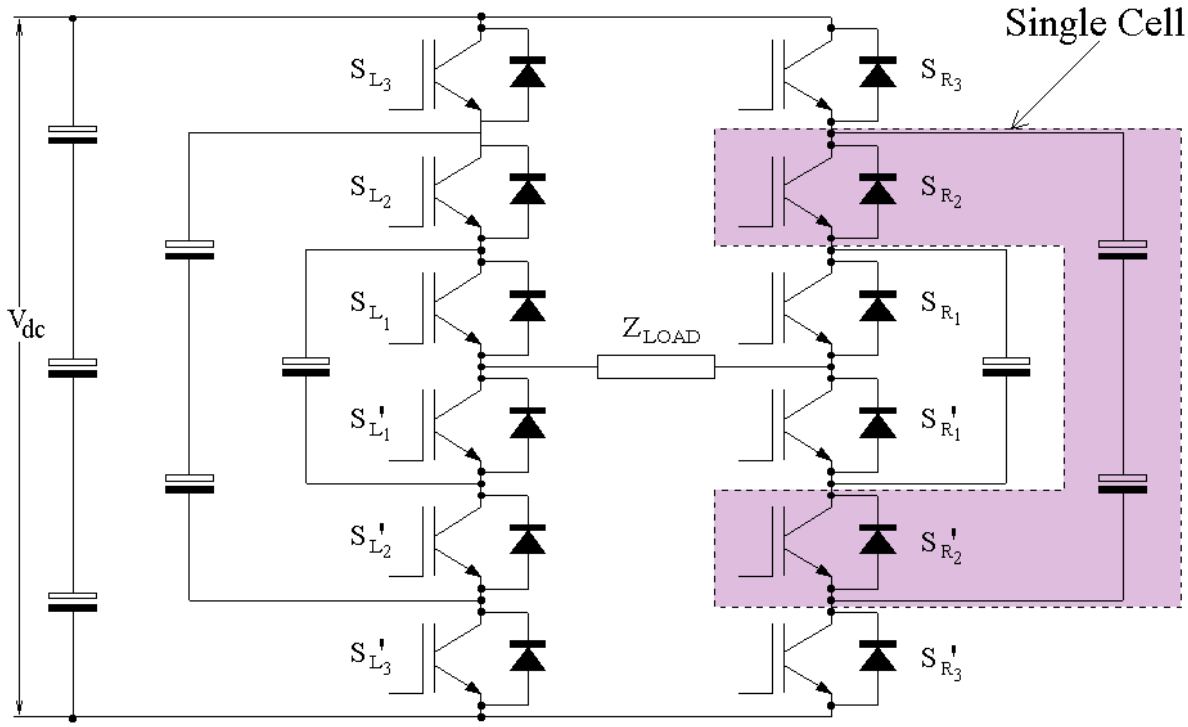

Figure 1: Three-Cell Inverter

This paper focuses on the flying-capacitor multilevel inverter used for synthesising approximated sinusoidal load voltages using staircase angle commutation control. The basic operation is described and a mathematical model is used to investigate all switching permutations. It is shown that the sizing of the cell-capacitors and selected switching sequence can be optimised to minimise the output harmonic distortion.

Basic Circuit Operation

The flying-capacitor inverter can be constructed to give an unlimited number of voltage levels, but for practical designs they are normally limited to six levels. The number of possible voltage levels is related to the number of power switching devices connected in series in each inverter limb. The circuit topology's inverter limb is in the form of a series of connected cells nested inwardly toward the load from the dc-link. Each cell, shown highlighted in Figure 1, has a capacitor and two power switches each comprising a transistor with an anti-parallel diode and operated in a complementary manner. In an N-cell inverter, each limb has 2N switches and applies N+1 distinct dc voltage levels from zero to V_{dc} across the load. The single-phase inverter full-bridge can also apply negative voltage levels across the load and so an N-cell inverter has 2N+1 distinct voltage levels. In a balanced inverter, the floating cell-capacitor average voltages are kept at multiples of the V_{dc}/N. The capacitor associated with the complementary switch pair nearest the load terminal will have the lowest voltage (V_{dc}/N), while the highest voltage ($(N-1)V_{dc}/N$) capacitor is associated with switches connected to V_{dc}.

The voltage contribution of each half-limb will depend on the number of switches in conduction in its upper portion. Therefore with *m* switches in conduction, the m^{th} voltage level is applied at the load terminal with respect to zero. The full load voltage is the difference between the left and right half-limb voltage levels. This voltage can be expressed as

$$V_{load} = \frac{V_{dc}}{N} \times \left(\sum_{n=1}^{N} S_{L_n} - \sum_{n=1}^{N} S_{R_n} \right) \qquad \text{... (1)}$$

where S_{Ln} and S_{Rn} ($n=1,2,\ldots N$) represent the left and right half-limb cell switch states, respectively, and logic '1' represents the upper switch in conduction and the lower switch in its blocking state.

Capacitor Voltage Balancing

One of the main reasons for using the multilevel flying-capacitor inverter is to operate at voltages higher than the individual power switch blocking capability. Safe operation entails keeping the cell-capacitor voltage differences within restricted voltage bands and so the capacitor voltages are balanced. The flying-capacitor inverter can operate with inherent capacitor voltage balancing, so long as the control utilises all the modes of charging and discharging at an intermediary voltage level [7, 8]. Figure 2 shows all the possible current paths for one cell-capacitor.

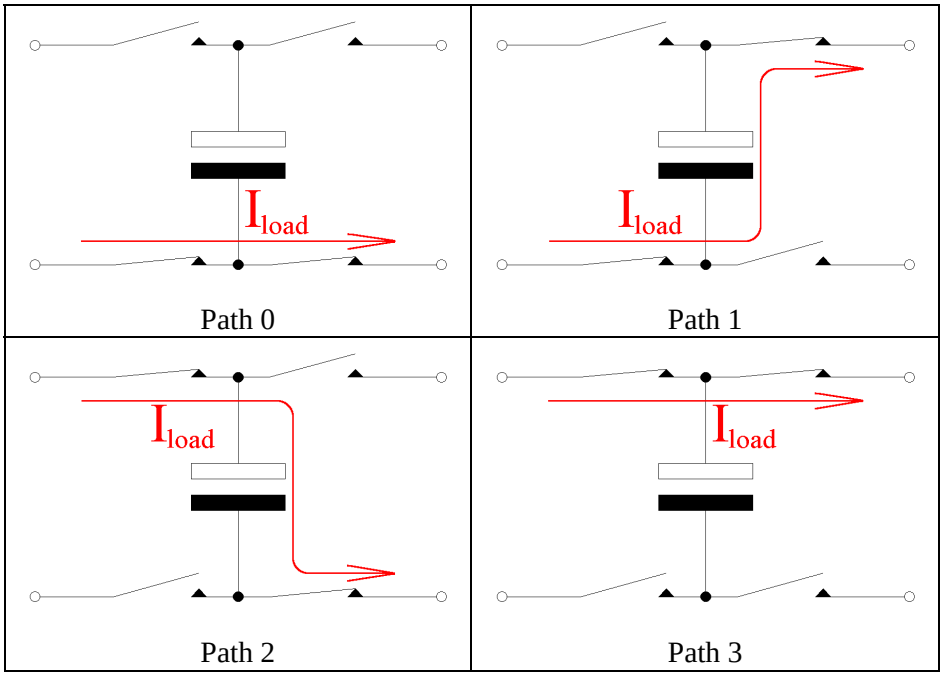

Figure 2: Cell-Capacitor Current Paths

The paths 0 and 3, and the paths 1 and 2 form complementary pairs where their correct usage can ensure capacitor voltage balancing and power loss sharing. In the steady state, paths 1 and 2 used over consecutive cycles will balance the capacitor voltage and device losses, as long as the operating period coincides with the same angular position in the cycle. This will lead to no net change in the charge on the capacitor, since the current integrals for each path would be equal and of opposite polarity. In the case of paths 0 and 3, their complementary usage must entail angular periods where the current is of equal and opposite polarity, thus ensuring the losses in each power device are the same.

Circuit Mathematical Model

The fundamental operation and characteristics of the flying-capacitor inverter can offer a great deal of flexibility in terms of operating modes compared to conventional two-level bridges. Complexity increases dramatically as the number of levels increases, and this makes it difficult to analyse the circuit's operation. Therefore, a simple mathematical model is developed which can assist circuit analysis under different switch states.

The mathematical equations for the inverter are constructed by expressing the rate of change of cell capacitor voltage, the output load voltage and current for all valid switching states. The equations are in a generalised form applicable to any N-cell inverter and the power switch states are included

separately. Thus the matrix form of the model for a generalised inverter half-limb (chopper) with an R-L load, shown in Figure 3, is as given below:

$$\frac{d[V]}{dt} = -[C]\times[A]^T \times[S]\times i_0 \quad \ldots (2)$$

$$v_o = \left[[S]^T \times[A]\right]\times[V] \quad \ldots (3)$$

$$\frac{di_o}{dt} = \frac{1}{L}\left(v_o - Ri_o\right) \quad \ldots (4)$$

where,

$$V = \begin{bmatrix} v_{C_n} \\ v_{C_{n-1}} \\ \ldots \\ v_{C_2} \\ v_{C_1} \end{bmatrix}, \qquad S = \begin{bmatrix} S_n \\ S_{n-1} \\ \ldots \\ S_2 \\ S_1 \end{bmatrix},$$

$$A = \begin{bmatrix} 1 & -1 & 0 & 0 & \ldots \\ 0 & 1 & -1 & \ldots & 0 \\ 0 & 0 & \ldots & -1 & 0 \\ 0 & \ldots & 0 & 1 & -1 \\ \ldots & 0 & 0 & 0 & 1 \end{bmatrix}, \qquad C = \begin{bmatrix} 1/C_n & 0 & 0 & 0 & \ldots \\ 0 & 1/C_{n-1} & 0 & \ldots & 0 \\ 0 & 0 & \ldots & 0 & 0 \\ 0 & \ldots & 0 & 1/C_2 & 0 \\ \ldots & 0 & 0 & 0 & 1/C_1 \end{bmatrix}$$

and,

V is the individual cell capacitor voltage vector and $v_{C_n} = V_{dc}$

S is the mode switch state vector where 1 indicates the high-side switch conducting and 0 the low-side switch conducting for each cell complementary pair.

Equation (4) represents the load characteristic and so be modified to represent other types of load.

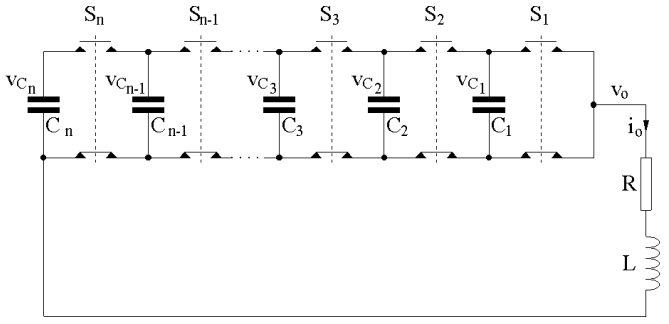

Figure 3: N-level Flying Capacitor Chopper

The above matrix relationships governing the flying-capacitor inverter can be incorporated within a simple fixed time-stepping procedure to calculate the load voltage v_o and current i_o with a particular switch state operated over a specific time period. By combining different switch states operated over different time-periods any switching sequence pattern can be simulated efficiently. This feature is very useful for analysing the inverter's operation when synthesising a sinusoid using a fixed control switching sequence. For example in a three-cell, single-phase inverter the A and C matrices are as follows:

$$A = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \quad \text{and} \quad C = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 2/C_c & 0 \\ 0 & 0 & 1/C_c \end{bmatrix}$$

where C_c is the basic cell capacitance.

By solving equations (1), (2) and (3) by iteration, the complete output load waveforms can be found for a given switching mode as defined by *S*.

Switching Control Strategy

To synthesise a sinusoidal waveform the flexibility of the multiple voltage levels allows simple staircase control, whereby each voltage level is applied across the load at a predefined electrical angle in a fundamental cycle. The quality of the output voltage is an important criterion in selecting the control angles. These angles are defined, in general, to give a low level of total harmonic distortion (THD) whilst achieving the desired fundamental amplitude. In addition for three-phase applications, the magnitudes of low-order harmonics should be low.

Furthermore the control must decide on which switching state to select at each voltage level since for a flying-capacitor inverter there are more than one switching modes available for the same intermediate voltage levels. The selection should obey the following three conditions:

- Allowing one independent switch changing state per voltage transition
- Maintaining capacitor voltage balancing
- Maintaining equivalent switching device usage

Thus for the three-cell inverter given above, one complete staircase cycle could employ the following sequence of switch states:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \Rightarrow \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \Rightarrow \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} \Rightarrow \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \Rightarrow \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \Rightarrow \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \Rightarrow \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

A series of modelling runs were conducted with all the possible bipolar sequences that give a balanced inverter operation in terms of the criterion listed above. There are 72 possible permutations that satisfy these conditions. Each produces an output voltage waveform with a different THD characteristic. Whilst the one giving lowest THD is naturally preferred, the control must ensure the voltages across the cell-capacitors are constrained within the range defined by the device blocking voltage rating. Simulation studies on all 72 switching patterns were carried out to analyse these issues.

The staircase transition angles were computed for a fundamental amplitude of 0.9 times the dc-link voltage, and with the 5th and 7th order harmonics eliminated. In this three-cell, single-phase case three angles and hence three harmonic amplitudes can be controlled, since the even harmonics in each half-limb's centre point voltage with respect to 0V are cancelled in the load voltage. In a three-phase system, this is not the case and only one angle and therefore only one load frequency component can be controlled in a three-cell inverter.

A load of 5Ω and 15mH in series was used in the simulation to represent a 600kW load and the 50Hz inverter dc-link was set to 3000V. The typical load waveforms for a 2700V peak, (≈2000Vrms) fundamental amplitude synthesised voltage with the cell-capacitor voltages superimposed are shown in Figure 4 with an individual cell-capacitor of 8200μF. The waveforms are displayed over three

cycles to illustrate the inherent capacitor voltage balancing of the switching state sequence used. The voltage between each cell-capacitor is the blocking voltage seen by the individual power switches and will increase as the cell-capacitance is reduced. In this particular example, the maximum voltage blocking requirement is 1400V with 8200µF, which is achievable with the latest 1700V IGBTs.

Figure 5 displays the spectrum of the load voltage waveform. Due to the balancing sequence repeating every three cycles, there are sub-harmonics present at multiples of a 1/3rd of the fundamental and these are included in the THD calculation.

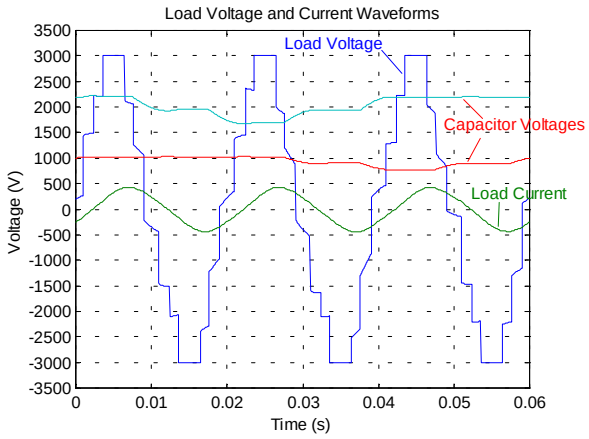

Figure 4: Load Waveforms - Low THD

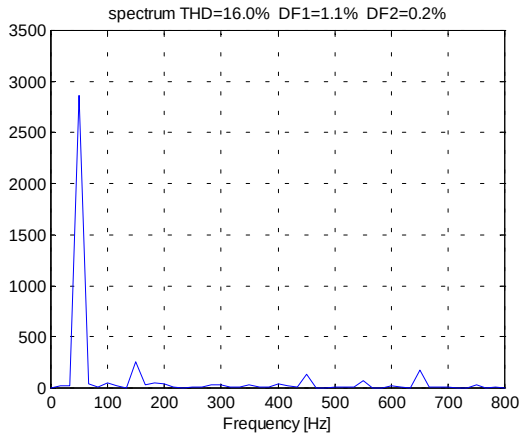

Figure 5: Load Voltage Spectrum - Low THD

The example load waveforms were produced for one particular switching state sequence that gives the lowest THD characteristic for the 8200µF cell-capacitance. There is a spread of THD characteristics for the different switching patterns and certain patterns cause an increase in the harmonics of the waveform as the capacitance reduces, while others cause the opposite affect. The highest level output THD switching pattern results are shown in Figures 6 and 7. The main factor distorting the output voltage in this case is the increased sub-harmonic content seen clearly in the voltage spectrum.

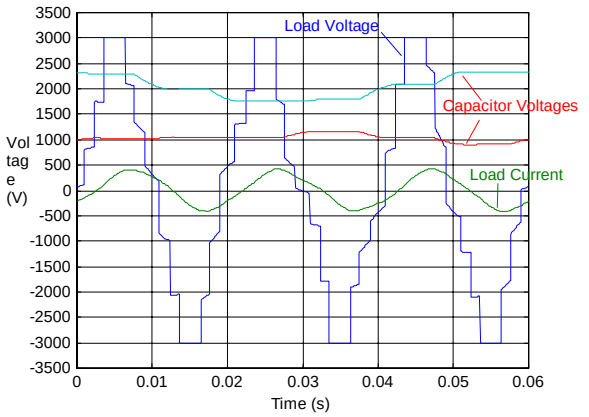

Figure 6: Load Waveforms - High THD

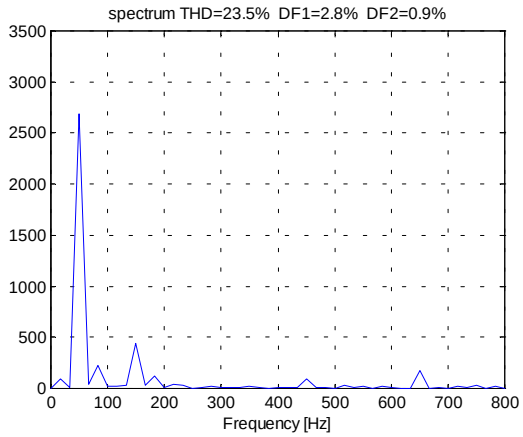

Figure 7: Load Voltage Spectrum - High THD

Figure 8 illustrates the variation in THD with cell-capacitance for the switching patterns producing the lowest and highest THD characteristic. This clearly indicates that the selection of switching state sequence can have a significant effect on output voltage quality. In the case of the 8200µF capacitor, the THD can be 50% greater if the wrong sequence is employed. Optimal control requires the lower THD switching pattern. This can be achieved by either pre-storing the pattern in the controller and running open-loop or using a routing algorithm which identifies the optimal pattern by using the computed output THD as a feedback variable.

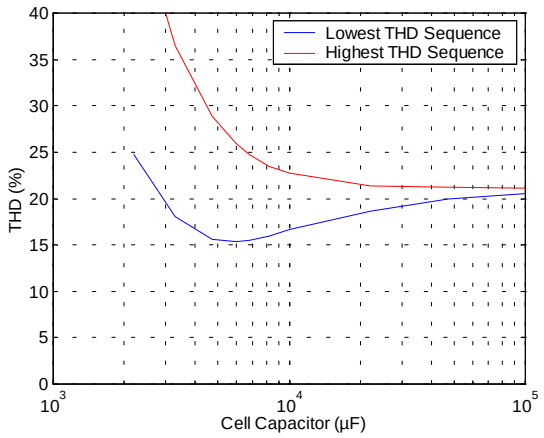

Figure 6: Switching Pattern THD Variation With Cell-Capacitance

The control should also monitor the cell-capacitor voltages, since this will affect operation. Under conditions where the voltages are within normal operating bands, the optimum switching pattern can be followed in sequence. If any of the voltages stray outside these bands, then the position within the switching sequence pattern will need to be reset to a point which will lead to the corrective charging function for the out of bounds capacitor voltage. This is important in a real system where the power device safe-operating regions must be observed.

Simulation Results

The matrix equation-based mathematical model of the flying-capacitor inverter is very useful for investigating and simulating the fundamental operation with various simple switching sequence control schemes. In order to validate the results of the modelling, a separate Simulink® simulation model of the flying-capacitor inverter has been developed. It makes use of the Power Systems Blockset add-on, which has various power electronic devices and machines models. This simulates a more realistic inverter with the effects of real power switches incorporated within the simulation. An individual power cell schematic is shown in Figure 9. The power switch parameters are selected to simulate a Semikron SKM500GA174D 1700V, 500A single IGBT. The Simulink® blockset model simulates this device as a fixed on-state voltage together with a low resistance when the gate signal is ‘1’ and as a high impedance when it is ‘0’.

The three-cell simulation results for the lowest THD switching sequence pattern identified by the modelling work are shown in Figures 10 and 11. The load and cell-capacitor waveforms look identical to those obtained by solving the matrix equations in the time-stepped model. The harmonic spectrum is also very close to that obtained by the modelling and the increase in THD value is entirely due to the reduction in fundamental amplitude caused by the power device voltage drops.

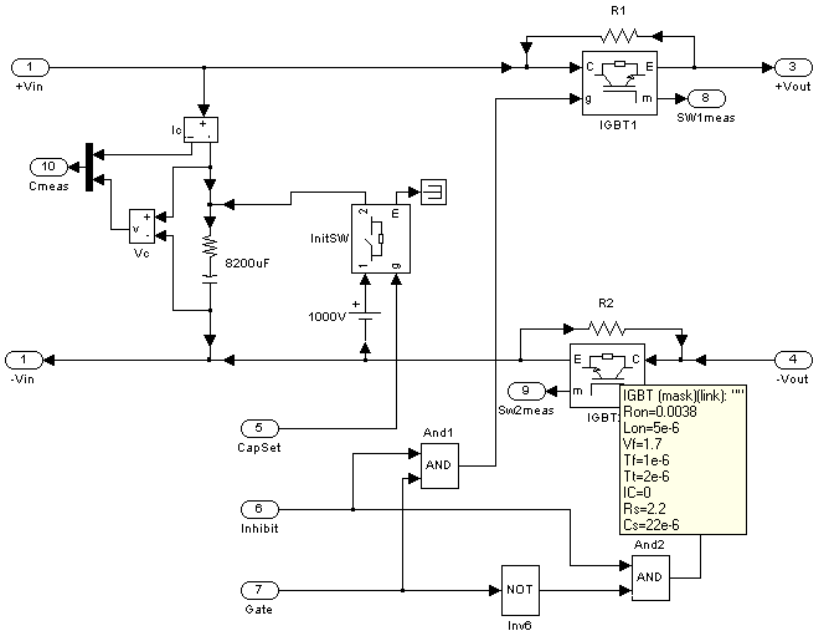

Figure 9: Inverter Cell Simulation Schematic

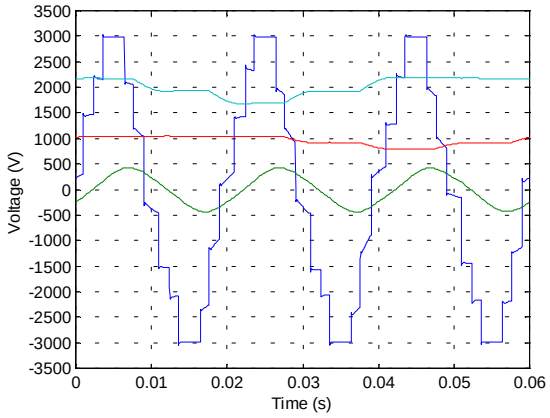

Figure 10: Simulation Load Waveforms

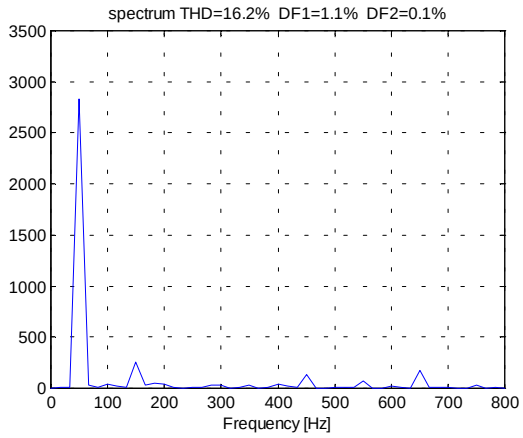

Figure 11: Simulation Voltage Spectrum

Conclusions

A flying-capacitor inverter can offer good power quality performance, with an economic number of power devices and capacitors, when operated in staircase angle control. A system model has been presented which allows for fast modelling and selection of the optimal staircase firing sequence. Circuit simulation has confirmed the validity of the model since the construction of an experimental very high power inverter is unrealistic. Modelling can identify the best capacitor size for cost and output performance and the firing control sequence can then be incorporated within the controller. Alternatively, the control system can operate in a self-tuning mode, whereby the control sequence permutations are tried-out in turn with the controller monitoring the output voltage and performing the THD calculation on-line. Future work will investigate further the requirements of the flying-capacitor inverter control in terms of capacitor balancing and minimising power device losses. Analysis of the impact of different switching sequences on the dynamic behaviour of the capacitor voltage balancing will lead to the development of an optimal control strategy for the inverter operating under transient conditions. Finally, a small scale working inverter will be constructed to test out the conclusions of the work in practice.

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