INFLUENCE OF MULTILEVEL SINUSOIDAL PWM SCHEMES ON THE PERFORMANCE OF A FLYING-CAPACITOR INVERTER

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ABSTRACT

Multilevel inverters, including the flying-capacitor topology require more complex control due to the additional flexibility offered by the multiple output voltage levels. One such control method is based on the conventional sinusoidal pulse width modulation (SPWM) scheme and uses multiple triangular carriers. There are a number of SPWM variants that achieve the desired inverter control. This paper presents the results of an investigation into these different schemes and their influence on the power quality and efficiency of a flying-capacitor inverter.

INTRODUCTION

The flying-capacitor inverter, first proposed by Meynard and Foch (1, 2), is a multiple voltage level inverter topology intended for high-power, high-voltage power applications. For instance, future large variable speed motor drives and static power conditioners for renewal energy distributed power systems will be practical using the flying-capacitor inverter. In common with all types of multilevel inverter, their main benefits lie in the utilisation of lower voltage power devices and the ability to synthesise a sinusoidal output with low harmonic distortion. The control for a multilevel inverter is more complex than a conventional bridge inverter, but the techniques employed are fundamentally the same. The additional voltage levels available to the load can be optimally used to improve the power quality at a reduced switching frequency. Control techniques such as staircase angle control (3), sinusoidal pulse width modulation (SPWM) and space vector PWM all offer solutions to the controller needs. Practical consideration must also be addressed to the need to balance power device utilisation and in the case of the flying-capacitor inverter, balance the cell-capacitor voltages. This paper presents an investigation into the performance of a practical flying-capacitor three-phase inverter supplying a star-connected lagging load when controlled by various SPWM schemes.

The flying-capacitor inverter employs capacitors within its structure in order to constrain the maximum voltages seen by each power switch. The topology is scalable in terms of voltage level, and a circuit is configured from a basic cell comprising a capacitor and two power switches operating in a complementary manner. Figure 1 shows the four-cell, three-phase inverter used in this investigation. The capacitor clamping feature presents a problem for the inverter control due to the need to ensure adequate capacitor voltage balancing under all operating conditions. Carrère et al (4) have shown that this issue can be addressed by utilising all the different switching states within the control. In an N-cell inverter, there are N possible switching states that supply the lowest voltage level. To ensure capacitor voltage balancing, all of these switching states must be used in equal measure in terms of period and cycle angular instance during steady state operation. This can be achieved by cycling each switching state in turn over N cycles for an N-cell inverter.

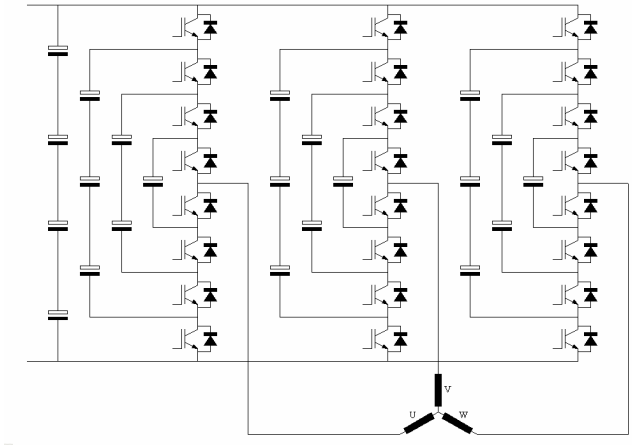

Figure 1: Four-cell, three-phase flying-capacitor inverter

SPWM CONTROL SCHEMES

Conventional two-level inverters are commonly controlled to give a sinusoid output voltage using a sinusoidal or sine-triangle PWM control scheme (5). The power device firing control signal is produced by comparing a triangular carrier with the desired sinusoidal voltage reference. Digital implementation of SPWM has lead to the adoption of asymmetric sampling where the reference level to be compared is

sampled at both the peak and trough of the carrier triangular signal. This technique can be applied to multilevel inverters by using multiple carriers and combining the resultant output control signals to set the applied voltage level and hence the inverter switch state. The two common forms of multicarrier scheme have either carrier disposition where each carrier occupies a specific voltage level band or carrier phase shifting in which each carrier occupies the same voltage band but at different phases. Figure 2 illustrates the basic phase disposition (PD) and phase shifted (PS) multicarrier techniques. The frequency modulation index, m_f, is selected to be a multiple of three, so that triplen harmonic cancellation takes place across the three-phase inverter load. Note that the effective inverter switching frequency of the PS scheme is higher by a factor of N, where N is the number of inverter cells.

Agelidis and Calais (6) have reviewed a number of variant forms of multicarrier SPWM. Phase opposition disposition (POD) and alternative phase opposition disposition (APOD) all have carriers occupying unique voltage bands but with inversion in lower half group (POD) or alternate inversion throughout (APOD). Another scheme, hybrid phase shifted (HPS), has two distinct groups of phase shifted carriers in the lower and upper regions of the reference. The reference signal can also be modified to include a 3rd harmonic component which will not appear across the load.

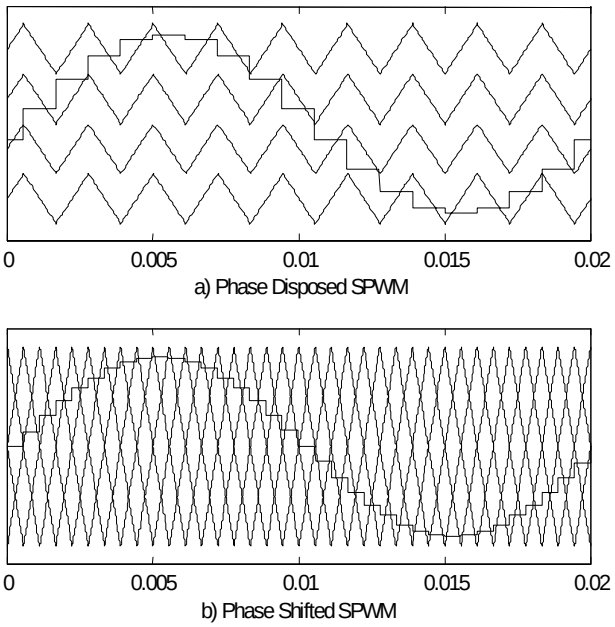

Figure 2: SPWM waveforms

CAPACITOR VOLTAGE BALANCING

It is important that inverter voltage switch modes are cycled to ensure cell-capacitor voltage balancing and equal device utilisation. This can be achieved in a SPWM controlled inverter by the addition of a simple logic circuit, shown in Figure 3, between the SPWM generation block and the gate drivers. N balance selection signals are required which only repeat after exactly N cycles, where N is the number of inverter cells. Only one balance signal is HIGH at any one time and the signal's mark must be longer than one complete PWM switching cycle (carrier period). The period is therefore an M^{th} of the total cycle period, where M is a prime number and is less than m_f. The balancing signals are latched at every combined switching transient in all the SPWM firing signals. The resultant signals are then used to route the SPWM signals via a multiplexer. This ensures that the original SPWM firing signals are swapped around the different inverter cells and that the same switching pattern is not repeated at the same angular position within the N balanced cycles.

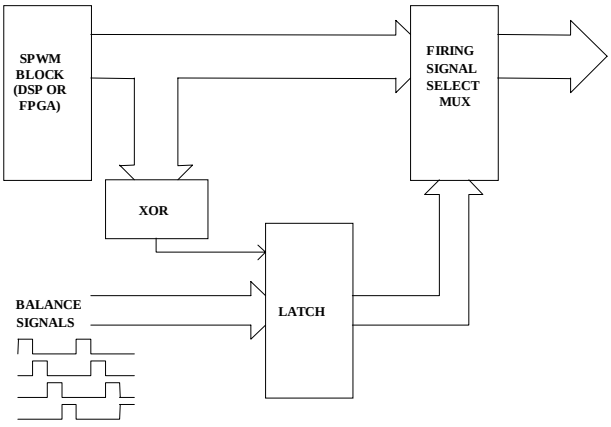

Figure 3: Inverter balancing logic

COMPUTER SIMULATION

The complexity of the control coupled with the effect of the capacitor voltage variation on the load voltage waveform means that computer simulation is required to fully evaluate the various merits of different SPWM schemes. A simulation program, written in C++, has been developed for carrying out a detailed simulation of an N-cell inverter, including the effect of the cell-capacitor voltage variations. Accurate models of IGBTs and diodes, using the manufacturers' published nonlinear conduction voltage drop and switching energy loss characteristics as a function of current, are included in the simulation program. The simulation uses a fixed time-step approach to solve the circuit voltages and currents. Device switching loss is

computed by summing the switching energy, based on the actual device current and voltage, at each device switching transition during the simulation run to get a total energy loss per simulation cycle. The control PWM generation uses an 8-bit triangular carrier in order to simulate a real digital implementation

The simulation of a 4 kV dc-link, four-cell, three-phase inverter using EUPEC 2.5 kV, 1000 A power modules is used for the investigations. The simulated load was set as a simple resistor (1.2 Ω) in series with an inductor (2 mH), giving a lagging power factor of around 0.85. With modulation amplitude set to 0.9, the load in each phase is approximately 1 MW.

Each simulation was allowed to run until the steady-state was reached. This typically occurs after 4 sinusoidal cycles for the simulated load time-constants used. Figure 4 shows the typical waveforms associated with SPWM control, in this case the PD scheme with a m_a = 0.9 (3600 Vpk) and m_f = 15 (750 Hz carrier frequency).

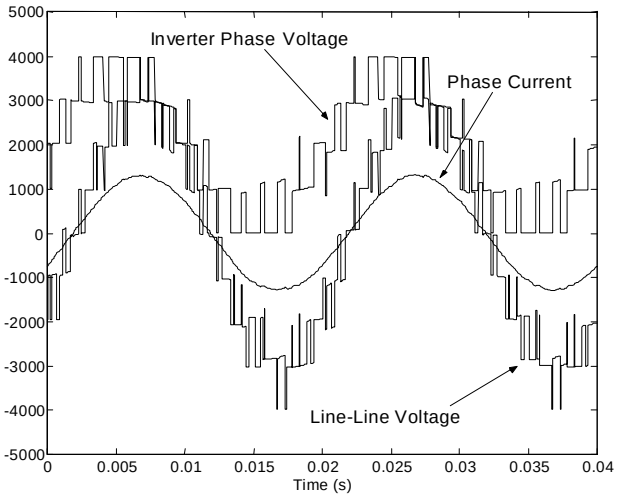

Figure 4: Inverter load waveforms

The individual capacitors' value will depend on the PWM switching frequency. In the simulations, the capacitance was selected to ensure that the voltage ripple on each cell does not exceed 10% of the nominal balanced voltage. Therefore, for a PWM switching frequency of 750 Hz, a 47000 μF capacitor is required. This ensures that the maximum voltage across each switch, which equals the voltage difference between adjacent cell-capacitors, does not exceed 1.5 kV. Figure 5 shows the cell-capacitor voltage waveforms for a complete balanced period of four sinusoidal output cycles. The effectiveness of the balancing control is confirmed since there is no net change in each voltage over the four cycles. Further confirmation of the correct system balancing can be seen in the device loss breakdown for one inverter limb detailed in Table 1. This shows that the conduction and switching losses are equally spread in each IGBT (SW1 - SW4). The losses in each diode (D1 - D4) are also roughly equivalent.

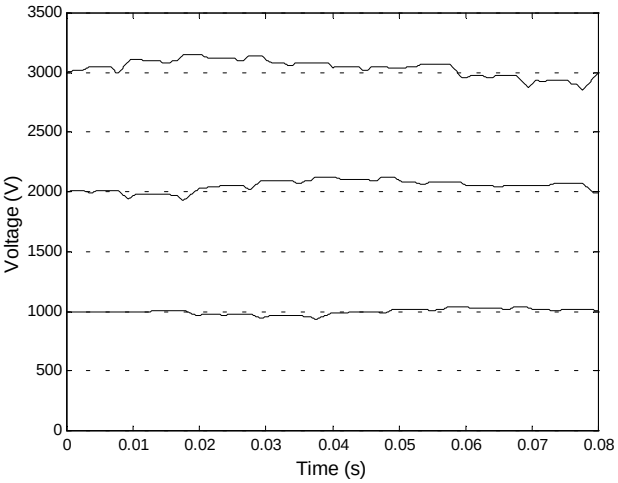

Figure 5: Cell-capacitor voltage waveforms (4 cycles)

TABLE 1 - Inverter loss breakdown (PD SPWM)

	Conduction (W)	**Switching (W)**
SW1 top	1327	233
SW1 bottom	1321	218
SW2 top	1329	246
SW2 bottom	1321	236
SW3 top	1328	232
SW3 bottom	1317	227
SW4 top	1328	227
SW4 bottom	1318	223
D1 top	163	137
D1 bottom	165	141
D2 top	163	137
D2 bottom	164	146
D3 top	165	137
D3 bottom	165	146
D4 top	165	138
D4 bottom	165	141
TOTAL	14869	

SPWM COMPARISON

In order to compare the different SPWM schemes, simulations were undertaken on the same inverter model as above and using the same modulation indices (m_f = 15 and m_a = 0.9). The spectrum of the line-to-line voltage for the PD, POD and PS control schemes are shown in Figure 6. These reveal that the PD scheme has a lower harmonic content than the other schemes. This is mainly due to the additional significant side bands present in POD and PS schemes. The APOD is very similar to POD but has slightly

lower amplitude harmonics either side of the PWM fundamental frequency (750 Hz). HPS is very similar to the PS scheme, but exhibits and are therefore not shown.

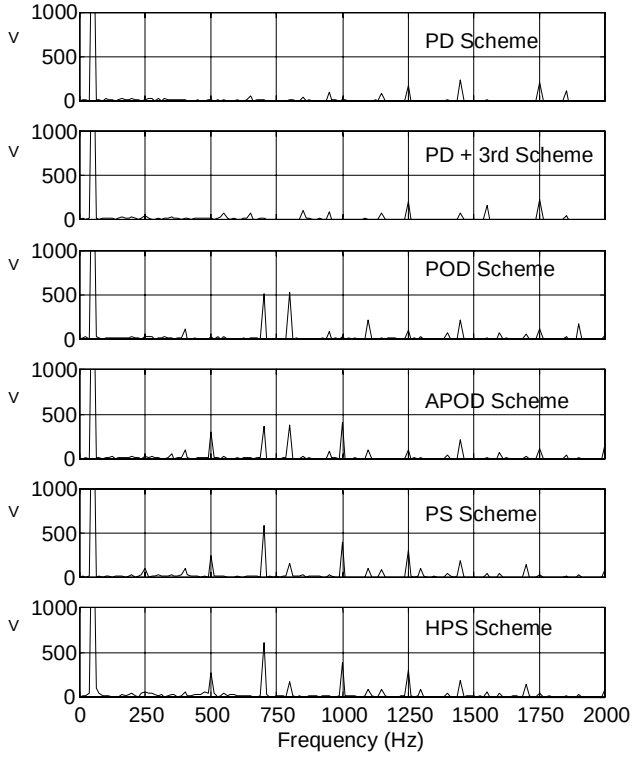

Figure 6: SPWM spectra comparison

To help quantify the quality of the waveforms the following indices are used (6):

Total Harmonic Distortion (THD)

$$THD = \frac{100}{V_1}\sqrt{\sum_{n\neq 1} V_n^2}\ \% \qquad \text{... (1)}$$

Distortion Factor 1 (DF1), applicable to AC motor drives (first order attenuation).

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n}\right)^2}\ \% \qquad \text{... (2)}$$

Distortion Factor 2 (DF2), applicable to UPS inverter stages and other AC supplies using a second order L-C filter.

$$DF2 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n^2}\right)^2}\ \% \qquad \text{... (3)}$$

Table 2 details the spectral quality of the different forms of SPWM investigated on the inverter with a m_a = 0.9 and m_f = 15. The individual capacitors are 47000 μF. Note that the PS and HPS schemes have scaled equivalent m_f values so that the switching frequency is the same in each case. It is clear that the PD scheme offers the lowest overall harmonic distortion, but the APOD scheme may be beneficial in static inverter systems, having the lowest DF2 figure. The results also indicate that it is beneficial to introduce a third harmonic component into the reference, which helps to slightly reduce the overall harmonic distortion. These distortion figures only indicate the harmonic content of the line to line voltage. Therefore, in a real application, the distortion in the current waveform should be compared, since it will include the filtering effect of the real load.

TABLE 2 - SPWM scheme spectral quality

	THD (%)	**DF1 (%)**	**DF2 (%)**
PD	19.48%	0.32%	0.09%
PD + 30% 3rd	19.00%	0.32%	0.09%
POD	31.72%	0.57%	0.12%
APOD	30.59%	0.50%	0.06%
PS	32.06%	0.59%	0.13%
HPS	33.98%	0.92%	0.21%

Variations in the positioning of the carrier waveforms in the PD case relative to the reference have also been investigated. The standard PD scheme is deemed a W-type where a peak in the carrier occurs at the reference peak. Alternatively, the carrier can be shifted by 180^o so that the trough coincides with the reference peak (M-type). Some work on this phase shift by Tolbert and Habetler (7) has suggested that there are some benefits in doing this. Therefore, simulations of carriers in 90^o offset steps were undertaken and the results are shown in Table 3. These indicate that a slight improvement in spectral quality can be achieved by phase shifting all the PD carriers. However, the potential for minimising the switching losses in the inverter was not shown in the simulation results. This result is based on accurate switching energy loss calculation, rather than based on the number of switching instances in one cycle. The balancing operation over four consecutive cycles also helps to smooth out any variations.

TABLE 3 - Carrier phase shifting PD scheme spectral quality

	THD (%)	**DF1 (%)**	**DF2 (%)**
PD	19.48%	0.32%	0.09%
PD + 90^o	18.74%	0.31%	0.07%
PD + 180^o	19.58%	0.37%	0.11%
PD + 270^o	18.75%	0.36%	0.07%

The typical inverter efficiency for all types of SPWM scheme is about the same at 98.6%. A detailed

comparison is contained in Table 4. Based on overall losses, there is relatively little to choose between the different schemes.

TABLE 4 - SPWM scheme power loss comparison

	P_{out} (kW)	P_{loss} (kW)	Efficiency (%)
PD	1018.6	14.87	98.54
PD + 90°	1012.8	14.59	98.56
PD + 180°	1021.9	14.78	98.55
PD + 270°	1021.8	14.46	98.59
PD + 30% 3rd Harm	1028.9	14.97	98.55
POD	1024.6	14.81	98.55
APOD	1024.0	14.82	98.55
PS	1027.4	14.70	98.57
HPS	993.4	14.11	98.58

The detailed loss breakdown also reveals that the balancing control scheme adopted works correctly on all schemes. Table 5 contains the mean and standard deviation of the IGBT and diode losses for each scheme. In most cases, the losses in the individual devices are within 2% of each other. The exceptions being the APOD and HPS schemes. The results also reveal that the PD scheme with a third harmonic added to the reference leads to the most evenly spread power device losses in the power converter.

TABLE 5 - SPWM scheme loss breakdown comparison

	IGBT		Diode	
	P_{mean}	Std. Dev.	P_{mean}	Std. Dev.
PD	1554	12.2	305	3.9
PD + 90°	1527	15.4	297	3.9
PD + 180°	1545	20.5	303	5.4
PD + 270°	1522	15.6	285	6.9
PD + 30% 3rd Harm	1559	5.1	312	2.8
POD	1549	14.2	303	3.8
APOD	1550	34.8	303	4.6
PS	1544	14.7	297	8.8
HPS	1488	50.7	276	51.0

SYSTEM PARAMETER OPTIMISATION

Choosing the best SPWM strategy can help minimise the harmonic distortion in the output waveform. Further improvements can be achieved by selecting the inverter capacitor value and the operational switching frequency, set by the m_f value. These parameters are interdependent since they both affect the capacitor voltage ripple and hence output voltage waveform. Figure 7 shows a three-dimensional plot of THD variations for different capacitance values and operating frequencies. The THD is lowest where the voltage ripple is lowest. A practical design must take into account the increased power losses associated with increasing the inverter frequency. Figure 8 illustrates the effect on varying the PWM carrier frequency. The capacitor selection will also be a compromise between performance and cost.

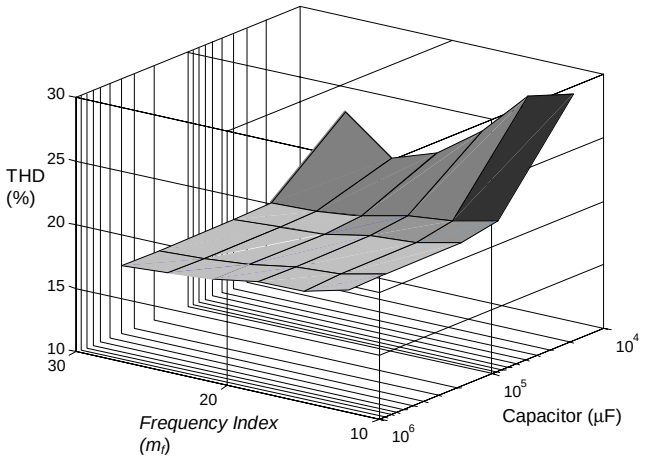

Figure 7: Variation of THD with frequency modulation index (m_f) and capacitance

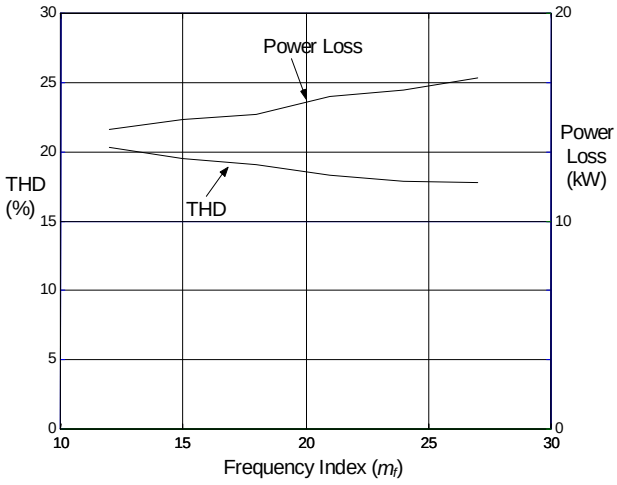

Figure 8: Loss and THD variation with frequency

CONCLUSIONS

The selection of a suitable SPWM strategy has been shown to be important in optimising the system performance of a flying-capacitor inverter. Although there are various forms of multicarrier SPWM, it has been shown that the phase disposed (PD) method with third harmonic injection offers the best solution for the flying-capacitor inverter when system balancing

control is employed. The simulation results also reveal that the inverter power losses are not dependent on SPWM strategy but are solely dependent on the switching frequency.

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