Control of Multilevel Flying Capacitor Inverters for High Performance

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Abstract -- **The paper presents a switching pattern selection scheme for the control of a multilevel flying capacitor inverter. The scheme reduces capacitor voltage fluctuation without using voltage feedback. The method is developed for sinusoidal voltage generation using the selective harmonic elimination (SHE) technique and was compared favorably with the result when voltage feedback was used.. The result of the comparison is presented. Simulation and experimental results from a four-cell five level flying capacitor inverter validates the method.**

Keywords – Flying Capacitor Inverter, Selective Harmonic elimination, THD

I. INTRODUCTION

The general function of multilevel converters is to synthesize a desired voltage from several levels of DC voltages. In contrast to their conventional two-level counterpart, their main advantage lies in reaching high voltage with low harmonics, using solid-state devices of lower voltage rating and much lower switching frequencies [1].

This paper explores the modulation strategies for flying-capacitor multilevel inverter. The four-cell five-level implementation of this circuit is shown in Fig. 1 [2, 3]. An important advantage of this circuit lies in having multiple switching combinations for the same voltage level. This gives flexibility in switching control strategies to achieve optimized output performance. Maintaining the correct voltage across the floating or cell-capacitor is the main challenge in ensuring proper operation of the inverter. Though it is desirable to use smaller capacitors in order to reduce cost and size of the inverter, the subsequent drawback is in the increased voltage swings on the intermediate voltage levels. This may cause excessive voltage stress on switching devices and the voltage ripple is counter-productive to producing a low harmonic content voltage waveform. A number of publications has addressed the issue of capacitor voltage balance [4,5,6].

The present paper investigates an optimal switching pattern selection mechanism for capacitor voltage balance without voltage feedback. The method is developed for sinusoidal voltage generation using the selective harmonic elimination (SHE) technique [7] and devices are switched only at or near fundamental frequency. The technique is intended for the control of high voltage static compensators. The paper discusses the principles applied for selecting the switching sequences. Simulation studies of the selected optimal pattern applied to the four-cell inverter circuit are presented. Comparison of the method with a capacitor voltage feedback scheme is also given. Simulation results demonstrate that the balanced capacitor voltages are obtained, and hence output line voltage/current THDs are significant reduced.

II. REVIEW OF SELECTIVE HARMONIC ELIMINATION SCHEME

The selective Harmonic Elimination (SHE) scheme is a well known PWM technique [7] in which the switching angles of the inverter are determined to set the fundamental voltage at some specific magnitude and simultaneously suppress certain harmonics. A multi-level inverter has the increased flexibility to synthesis its voltage waveform offered by the multiple voltage levels. In its simplest control form, the resultant waveform for the phase voltage of the inverter in Fig. 1 has the shape of a staircase shown in Fig. 2.

Notice that the number of controlled components is equal to half the number of cells in the inverter due to the requirement for symmetry around the mean level, with each inverter limb operated in bipolar mode. With basic SHE control, the four-cell, five-level inverter under investigation can only be controlled with the fundamental regulated and one harmonic eliminated yielding equations as must be solved using the Newton-Raphson method to obtain the required control angles

$$\cos(\alpha_1)+\cos(\alpha_2)=\frac{\pi m_a}{2} \quad (1)$$

$$\cos(5\alpha_1)+\cos(5\alpha_2)=0 \quad (2)$$

where α_1 and α_2 are the angles at which a level transition occurs. The Newton-Raphson method can be to solve the nonlinear equations (1) and (2) for the α_1 and α_2. Fig. 2 shows the resultant staircase shaped phase and line voltage waveforms when fundamental magnitude is set to 85%.

This method can be extended to higher orders of harmonic elimination, but obtaining a solution can be tedious and other approaches have been suggested [8].

The performance of the control schemes has been assessed using the total harmonic distortion (THD) and distortion factor 1 (DF1) [9] figures of merits. However as is known the balancing of a multilevel inverter can generate

significant sub- and inter-harmonic frequency components at multiples of the fundamental divided by the number inverter cells per phase [9]. To ensure that these components are not ignored, the THD and DF1 formulae have been modified as

$$THD = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} V_{i/m}^2 - V_1^2} \ \% \qquad (3)$$

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} \frac{m^2 V_{i/m}^2}{i^2} - V_1^2} \ \% \qquad (4)$$

to take into account the number of levels in a multilevel inverter.

In addition a parameter, the energy factor ξ, is defined in this study for assessing the performance of a control scheme with respect to the characteristics of a flying capacitor inverter

ξ relates the unit cell-capacitor stored energy to the total load power of the three-phase inverter and is given as

$$\xi = \frac{3}{4RC} \ \text{s}^{-1} \qquad (5)$$

Derivation of ξ is given in [10]. .In a practical system, the designer would aim to minimise the capacitor size leading inevitably to increased ripple on the capacitors voltages. So the parameter, ξ, needs to be as large as realistically possible, while maintaining safe operation of the inverter by minimising the peak switch blocking voltages and peak capacitor voltages. The ripple voltage will also be dependent on the amount of current flowing when the capacitors are in the load current path. Therefore, the current lag angle, ϕ, is also an instructive parameter when quantifying the inverter performance with the system design parameters.

III. Switching Pattern Selection

The rules for selecting the optimal switching patterns for voltage balance are as follows:

1. eliminate those switching patterns causing a capacitor to be charged and subsequently discharged, or vice versa, at peak current,

2. match the switching states in a cycle to ensure nil net charge accumulation in a capacitor.

The subsequent selection scheme is developed and tested using the four-cell five-level inverter as an example and can be extended to multilevel inverters of any number of levels.

A. Switching States and Sequences in a Four-Cell Inverter

In a four-cell chopper circuit shown in Fig. 3(a) which forms one phase limb of the three-phase flying capacitor inverter shown in Fig. 1, there are 16 distinct switching states. Table 1 lists all these switching states represented as 16 binary numbers and their corresponding net charging effect on each of the cell capacitors for a positive load current. The most significant bit of these binary numbers controls the outer complementary switch pair nearest the dc link (S_4). '1' indicates that the upper switch is in conduction and contributes to a net voltage level at the inverter output. As can be seen in the table, the switching states for the levels -0.5 and 0.5 all lead to different charging effects in the three cell-capacitors, hence causing the voltage swings.

In the case of the level 0 switching states, these can be grouped in three complementary pairs, considering the charging characteristic for all capacitors in this inverter. The complementary pairs are states 3 & C, states 5 & A and states 6 & 9.

Synthesizing a sinusoidal cycle using the SHE staircase requires the inverter stepping through a set of three intermediate states, i.e. a switching sequence, from voltage levels -1 to +1. Even though there are a large number of possible switching sequences, the number is limited to those with only one switch state transition per level change. This is to minimize the switching losses in the power semiconductors of a real inverter. The number of allowable transitions between switching states in the four-cell inverter is illustrated in Fig. 3(b). The figure shows that there are four possible paths between level -1 and a level -0.5, three possible paths between any level -0.5 and a level 0, two possible paths between any levels 0 and a level +0.5 and one possible path between any level +0.5 and level +1.

Therefore, 24 different sequences of switching states can be used when stepping-up in voltage level between -1 and +1. For instance, the switching states to be used in one cycle may be [0000], [0001], [1001], [1101] and [1111], so 0, 1, 9, D and F in hexadecimal notation. This switching sequence is labeled as $\overset{D}{9}_{1}$.

Using the above labeling, the 24 possible switching sequences are as follows:

$$\overset{7}{3}_{1}, \overset{B}{3}_{1}, \overset{7}{5}_{1}, \overset{D}{5}_{1}, \overset{B}{9}_{1}, \overset{D}{9}_{1}, \overset{7}{3}_{2}, \overset{B}{3}_{2}, \overset{7}{6}_{2}, \overset{E}{6}_{2}, \overset{B}{A}_{2}, \overset{E}{A}_{2}, \overset{7}{5}_{4}, \overset{D}{5}_{4}, \overset{7}{6}_{4}, \overset{E}{6}_{4}, \overset{D}{C}_{4}, \overset{E}{C}_{4}, \overset{B}{9}_{8},$$
$$\overset{D}{9}_{8}, \overset{B}{A}_{8}, \overset{E}{A}_{8}, \overset{D}{C}_{8}, \overset{E}{C}_{8}$$

B. Switching Patterns and Their Selection

A pattern refers to a set of four switching state sequences for voltage balancing over four cycles. To analyze the pattern selection problem, it is assumed load current is sinusoidal and the phase current lags the phase voltage fundamental component. Fig. 4 shows the relationship between the phase voltage and current under staircase SHE control. The figure also shows the component of load current which can flow through the cell-capacitors for 0 and 0.5 voltage levels. As can be seen from level 0 operation, the current is of equal amplitude but of opposite polarity in the two halves of the staircase voltage cycle, hence the mean current is zero. This means that under ideal conditions, the same switching state could be used throughout for level 0 synthesis However this strategy can not be employed for the reasons explained below. As shown in Fig. 4 (c), the current waveforms for level 0.5 are totally different for the two halves. There is no symmetry in the load current to exploit for balancing purposes when operating at level +0.5, so all four switching states for this level as shown in Fig. 4 have to be cycled through over four cycles.

One approach used in identifying valid balancing switching patterns is to keep the individual level switching states the same over one complete cycle, thus forming a sequence. According to three complimentary pairs of level 0 switching states, it is clear that there are groups of 6 pattern permutations made up of just 4 individual sequences, where the sequence order is varied. These groups of sequences are listed in Table 2, with the level 0 contributing states shown as reference. The basic requirement is that all four -0.5 and +0.5 level states are used, but the level 0 states can be taken from either one complementary pair set or two sets out of the six. Thus there are in fact 24 different groups of switching sequences, and by permutation each has 6 different patterns. So this gives a grand total of 144 valid balancing patterns that meet the minimum switching transition criteria. Taking the upper left group in Table 2 as an example, the 6 pattern permutations in this group are as follows:

$$\overset{7EDB}{36C9}_{1248},\ \overset{7EBD}{369C}_{1284},\ \overset{7DEB}{3C69}_{1428},\ \overset{7DBE}{3C96}_{1482},\ \overset{7BED}{396C}_{1824},\ \overset{7BDE}{39C6}_{1842}$$

Two rules have been devised to select a pattern out of 144 which will give the best performance. The first is to avoid those switching patterns which cause the same capacitor to be charged and subsequently discharged or vise versa at peak current. Fig. 5 shows that the phase current magnitude is maximum at levels -0.5 and +0.5. Hence these regions will have the largest levels of capacitor voltage variation. So if state 7[0111] is used at +0.5 level in the first sequence, voltage drop on C_3 would be the maximum due to the peak discharging current. On the other hand if the state 8[1000] is applied at -0.5 level in the subsequent sequence, C_3 would be charged with the most negative current causing further voltage drop. Thus if the switching state at level +0.5 gives the same polarity of voltage change as the next sequence's switching state at level -0.5, then this is to be avoided. Consequently preferred patterns should not include the next level -0.5 state being the 1's complement of the previous level +0.5 state. For instance, state 8 [1000] should not follow state 7 [0111]. According to this rule the following consecutive sequences pairs are not preferred: $\overset{7}{\underset{X}{X}}\ \overset{X}{\underset{8}{X}},\ \overset{E}{\underset{X}{X}}\ \overset{X}{\underset{1}{X}},\ \overset{D}{\underset{X}{X}}\ \overset{X}{\underset{2}{X}},\ \overset{B}{\underset{X}{X}}\ \overset{X}{\underset{4}{X}}$

The second rule considers the charging/discharging of capacitors within one sinusoidal cycle due to the switching sequence used. The aim is to ensure that a particular capacitor is in the same current path over this cycle, so that there is no or as little as possible net charge accumulation. As shown in Table 1, when adjacent switches are in the opposite state, the capacitor between them lies in the load current path, and so its voltage would swing. Again, with regard to the peak and trough of the current occurring around level +0.5 and level -0.5 respectively, it is preferable if as many cells as possible are in the same state at both levels. Priority for this rule can be assigned to the higher voltage capacitor, i.e. C_3, which will see the largest voltage change. For example if at level -0.5 the switching state is 4 [0100], then state 7 [0111] is preferred for level +0.5. In both sequences C_3 lies in the load current path and is in discharging mode. Fig. 6 shows the resultant current flowing through C_3. As can be seen, there is symmetry in the cell-capacitor current and so the mean current is zero leading to no net change in cell-capacitor voltage. Applying the same rule, states 8 [1000] and B [1011] are also preferred within a sequence as C_3 is in charging mode for both voltage stepping-up and down cases. Another condition applicable to state transitions within a sequence is that of only switching one cell transistor pair at a time. This means that only four sequences would be preferred for minimising the voltage variation on C_3 over one sequence cycle, and in each case C_3 is in the same current path throughout the cycle. These are:

$$\overset{7}{\underset{4}{5}},\ \overset{7}{\underset{4}{6}},\ \overset{B}{\underset{8}{9}} \text{ and } \overset{B}{\underset{8}{A}}$$

According to this rule there are 4 sequences, shown below, preferred within a pattern:

$$\overset{7}{\underset{4}{5}},\ \overset{7}{\underset{4}{6}},\ \overset{B}{\underset{8}{9}} \text{ and } \overset{B}{\underset{8}{A}}$$

When applying this second rule to C_2, and to C_1, states in the adjacent cells around C_3 must not be complements, otherwise the above rule will be broken. Therefore, this means that the following 4 sequences are preferred for use in a pattern:

$$\overset{D}{\underset{4}{5}},\ \overset{D}{\underset{4}{C}},\ \overset{E}{\underset{2}{6}} \text{ and } \overset{E}{\underset{2}{A}}$$

Applying the above two rules, one particular pattern for the four-cell five-level inverter is likely to be among those offering the best performance, viz:

$$\overset{7EDB}{36C9}_{1248} \qquad \textbf{PATTERN 1}$$

This pattern does not have any consecutive states which break the first rule governing the level +0.5 followed by level -0.5. It also contains 3 sequences from the second rule which have preferred state combinations for levels -0.5 and +0.5.

The various balancing patterns can also be screened for ones which are likely to cause poor overall performance. One such pattern which breaks the first rule only has one good sequence from the second rule for C_1 is as follows:

$$\overset{7BED}{3AC5}_{2841} \qquad \textbf{PATTERN 2}$$

The same rule-based analysis can be done for other load characteristics. In the case of a leading phase current angle, the second rule governing a sequence still applies, the first rule's reasoning is the same but applied this time to a sequence level -0.5 state followed by the next sequence level +0.5 state.

The overall pattern, thus derived, is repeated once every four cycles (number of cells), with different switch states used at the same voltage level of each cycle.

IV. Comparison Of Balanced Switching Patterns

Simulation results for switching patterns 1 and 2 identified in the previous section are presented in Table 3. These are also compared with the ideal case where constant capacitor voltages are assumed. The dc link voltage was set to 400 V and control settings were m_a = 1 and a fundamental frequency of 50 Hz, using 5th harmonic elimination angles for staircase SHE control. The phase voltage fundamental is therefore 141.4 V(rms) and the line

voltage fundamental is 244.9 V(rms). The load model used has component values R = 2.5 Ω and L = 7.958 mH, and the individual cell-capacitance is 10 mF. For these component values the energy factor, ξ, is 30 s^{-1} and the nominal output power for an equivalent ideal sinusoidal system is 12 kW with power factor 0.707.

As can be seen in Table 3, PATTERN 1, $(^{7\ E\ D\ B}_{3\ 6\ C\ 9\ 1\ 2\ 4\ 8})$, offers lower output waveform harmonic distortion compared to PATTERN 2, $(^{7\ B\ E\ D}_{3\ A\ C\ 5\ 2\ 8\ 4\ 1})$. The table also shows that by optimum pattern selection the phase and line voltage THDs can be lowered compared to the ideal case. However, because of the additional sub- and inter harmonics at the low frequency, phase current THD is higher. The DF1 term indicates good correlation in predicting the THD of the phase current for this particular simple inductive load.

Fig. 7(a) shows the line voltage spectrum for the two cases, with the frequency components normalised to the fundamental. PATTERN 1 gives lower THD level than its counterpart. Notice that a 12.5 Hz component is present in the voltage spectrum for both patterns and its magnitude is higher for the inferior PATTERN 2. This component is due to the balancing pattern control strategy which repeats every four cycles, i.e. 12.5 Hz.

Fig. 7(b) shows the individual cell-capacitor voltages, plotted on the same zero axis for reference, of the inverter controlled by the two balancing pattern schemes. With PATTERN 1, voltage ripple is reasonably low with blocking voltage variations peaking at ±50 % of the nominal values. However for PATTERN 2 capacitor voltage ripple is significantly higher with a peak blocking voltage value around 100% of the nominal level. This is the primary reason for PATTERN 2's poorer waveform performance.

V. Closed-Loop Capacitor Voltage Balancing

Capacitor voltage balance may be obtained by voltage feedback control method using voltage sensors. This is particularly valid in cases when the load parameters vary considerably within a cycle [11] There have been a number of proposed schemes for maintaining balanced regulation of the cell-capacitor voltages specifically under PWM control [12]. No work has been reported for balancing when using staircase SHE control and so an algorithm which will accomplish balanced operation is proposed in this section.

The proposed method employs comparators for an upper and lower voltage level band for each capacitor. Their output states are combined so that the signals for each capacitor are shown in Table III. This uses the relationship between the switch state of those mutually connected to a capacitor and charging/discharging behaviour dependency on current direction. For instance, an adjacent two cells' state of '10' with a positive phase current flowing will boost the voltage across the capacitor connected between the cells.

Using these comparator signals, a simple algorithm for a four-cell inverter can be implemented to decide the optimum switching state to apply to the inverter at a given level. A flow diagram of the algorithm is shown in Fig. 8. The algorithm input signals are the three comparator outputs C1 - 3 and the required output voltage level L. The state of the highest voltage capacitor is checked first. If it is within bands [0000], then the state of the middle capacitor is checked, otherwise the output firing switching state S is assigned to C3. If C2 is outside the regulation bands then S is assigned to C2. The comparator signal C1 for the lowest voltage capacitor is added to S only if the state of C2 is [0000]. This gives a potential switching state for the inverter control. If all three capacitor voltages are within the regulation bands, S = [0000], then the optimum pattern for the given voltage level demand is found using a look-up table. Otherwise, S is checked to ensure that it operate the inverter at the required voltage level. If this is not the case, S is either incremented of decremented until the switching state gives the appropriate voltage level.

Simulations were conducted under the same conditions as before and the resultant capacitor voltages are shown in Fig. 8, and compared with the optimum PATTERN 1 result. This shows that the voltage ripple has been reduced by applying feedback, but this appears to lead to a pseudo-random behaviour rather than a repeating waveform as before. The tolerance band was set at ±5%, and it was found that tighter tolerances caused instability in the simulation. The mean capacitor voltages were all kept within 3% of the target values, and the peak voltages were reduced compared with PATTERN 1. For instance, peak voltage on C_3 as a percentage of the unit cell-voltage was 318.2% compared to 332.3%. These show that the algorithm is achieving balanced voltage control with reduced ripple even compared with the optimum selected pattern. The maximum blocking voltage as a percentage of unit cell-voltage across any switch was also reduced to 156.4%, compared to 167.8% for PATTERN 1. This shows that some improvement can be gained in protecting against over-voltage conditions across the power switch, or it may be possible to increase output power for a given cell-capacitance.

The effect of the change in capacitor voltage on output power quality is shown in the plots of line voltage and phase current spectra. For comparison, the PATTERN 1 spectra are also shown in Figs. 9 and 10. The most interesting feature in the harmonics is a general increase in the sub- and inter-harmonics, but the 100 Hz component is noticeably reduced. This is due to the more random nature of the capacitor ripple waveform effectively spreading the spectral components. This is reflected in increased line voltage and phase current THD, but the values are still lower than a poorly selected open-loop balancing pattern. These results indicate that under steady-state conditions, the pre-selected balancing pattern is preferred due its lower harmonic distortion characteristic, but in a real system the closed-loop cell-capacitor voltage control would ensure better transient operation.

VI. Conclusions

The paper presented an optimal capacitor voltage balancing strategy using a selective harmonic elimination scheme. Switching states for a three-phase four-level flying capacitor inverter were investigated. Criteria have been identified to choose the switching sequence/patterns which would cause least disturbances to the capacitor voltages.

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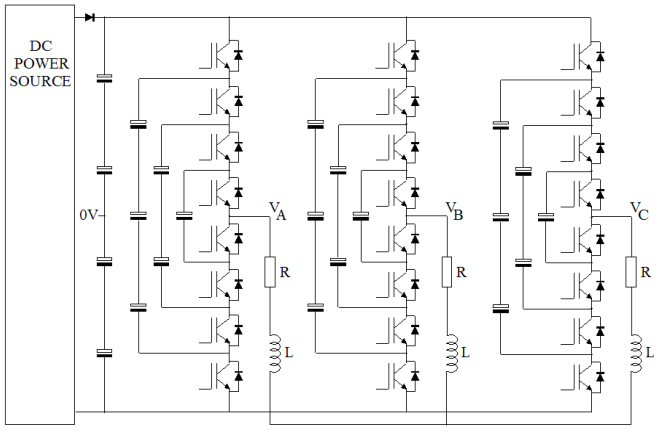

Figure 1. Five-level flying-capacitor inverter circuit

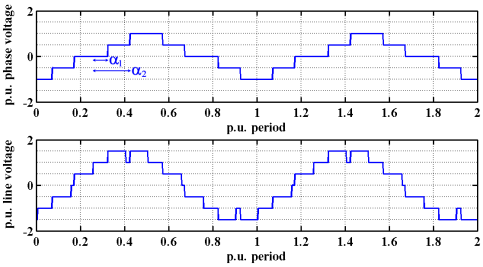

Figure 2. Idealized phase V/I waveforms with 45° lagging current

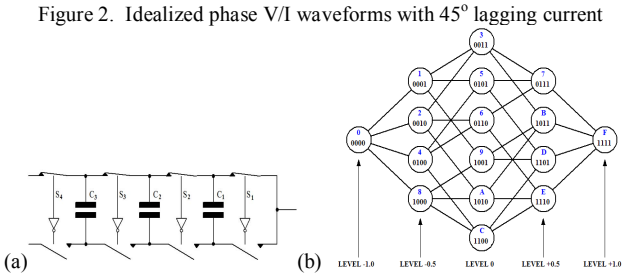

Figure 3. Simple four-cell chopper circuit and its allowable transitions between level

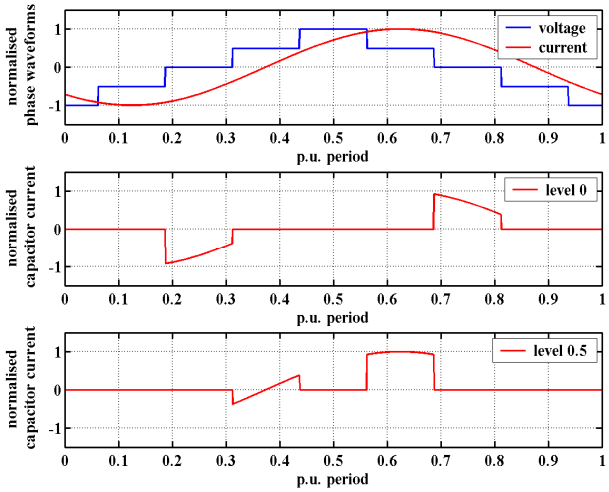

Figure 4. Idealised phase current and voltage waveform with 45° lagging current

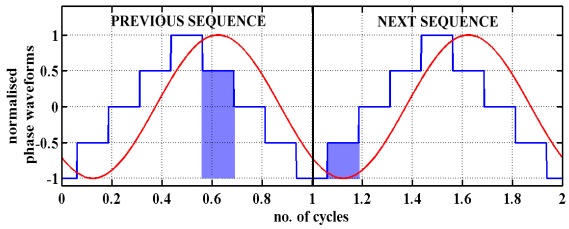

Figure 5. Switching patterns causing large voltage swings should be avoided

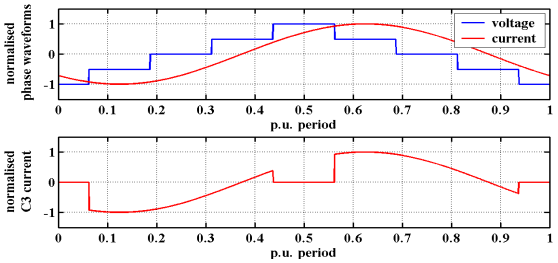

Figure 6. Current flowing through C_3 when using switching sequence 4,7,5

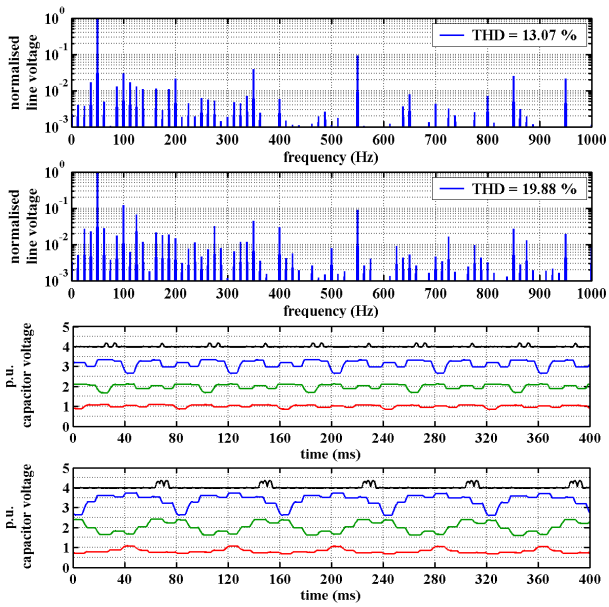

Figure 7. Comparison of Line voltage spectrum and capacitor voltages PATTERN 1 (top) and PATTERN 2 (bottom)

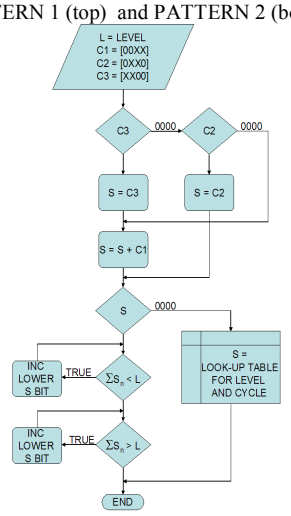

Figure 8. Flow chart for closed-loop voltage regulation

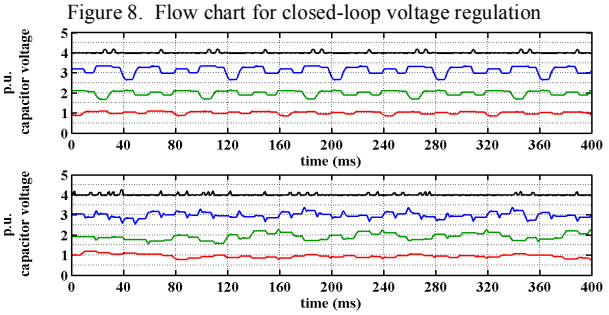

Figure 9. Capacitor voltage ripple, PATTERN 1 (top) and closed-loop regulated capacitor voltage (bottom)

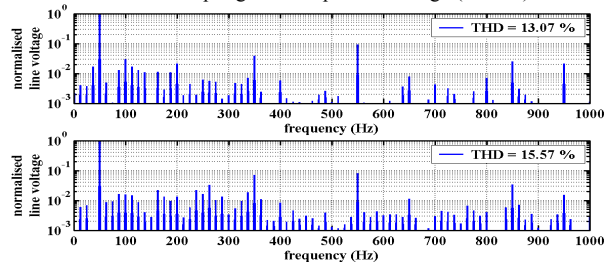

Figure10. Line voltage spectrum comparison, PATTERN 1 (top) and closed-loop regulated capacitor voltage (bottom)

TABLE I
CAPACITOR VOLTAGE NET CHANGE
FOR EACH INVERTER LIMB SWITCHING STATE

Switching State $S_4S_3S_2S_1$	Output Voltage Level	Change(+VE)/ discharge(-VE) C_3	Change(+VE)/ discharge(-VE) C_2	Change(+VE)/ discharge(-VE) C_1
0000 (0)	-1.0			
0001 (1)	-0.5			-VE
0010 (2)	-0.5		-VE	+VE
0100 (4)	-0.5	-VE	+VE	
1000 (8)	-0.5	+VE		
0011 (3)	0		-VE	
0101 (5)	0	-VE	+VE	-VE
0110 (6)	0	-VE		+VE
1001 (9)	0	+VE		-VE
1010 (A)	0	+VE	-VE	+VE
1100 (C)	0		+VE	
0111 (7)	+0.5	-VE		
1011 (B)	+0.5	+VE	-VE	
1101 (D)	+0.5		-VE	+VE
1110 (E)	+0.5			-VE
1111 (F)	+1.0			

TABLE II
24 GROUPS OF SWITCHING SEQUENCES

Level 0	Switching Sequence Groups			
3+C and 6+9	7 E D B 3, 6, C, 9 1 2 4 8	B 7 E D 3, 6, C, 9 1 2 4 8	D B 7 E 9, 3, 6, C 1 2 4 8	D B 7 E 9, 3, 6, C 1 2 4 8
3+C and 5+A	7 B D E 3, A, 5, C 1 2 4 8	B E 7 D 3, A, 5, C 1 2 4 8	7 B D E 5, 3, C, A 1 2 4 8	D 7 E B 5, 3, C, A 1 2 4 8
6+9 and 5+A	7 B E D 5, A, 6, 9 1 2 4 8	D E 7 B 5, A, 6, 9 1 2 4 8	B 7 D E 9, 6, 5, A 1 2 4 8	D E 7 B 9, 6, 5, A 1 2 4 8
3+C	7 B D E 3, 3, C, C 1 2 4 8	7 B E D 3, 3, C, C 1 2 4 8	B 7 D E 3, 3, C, C 1 2 4 8	B 7 E D 3, 3, C, C 1 2 4 8
5+A	7 B D E 5, A, 5, A 1 2 4 8	7 E D B 5, A, 5, A 1 2 4 8	D B 7 E 5, A, 5, A 1 2 4 8	D E 7 B 5, A, 5, A 1 2 4 8
6+9	B 7 E D 9, 6, 6, 9 1 2 4 8	B E 7 D 9, 6, 6, 9 1 2 4 8	D 7 E B 9, 6, 6, 9 1 2 4 8	D E 7 B 9, 6, 6, 9 1 2 4 8

TABLE III
TRUTH TABLE FOR CAPACITOR VOLTAGE COMPARATORS

Capacitor	Over-voltage Condition		Under-voltage Condition	
	Positive Current	Negative Current	Positive Current	Negative Current
C_3	0100	1000	1000	0100
C_2	0010	0100	0100	0010
C_1	0001	0010	0010	0001