# Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection

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**Abstract:** A rule-based scheme is investigated for capacitor voltage balancing in a multilevel flying capacitor inverter (MFCI). Without using voltage feedback, the scheme determines the best switching pattern for maintaining nil mean current in all capacitors, hence minimising the capacitor voltage fluctuation. The method is developed to work with the selective harmonic elimination (SHE) technique for sinusoidal voltage generation applied to control static VAR compensators. The method has been designed using a four-cell five-level MFCI as an example. The selected pattern has been shown to give superior performance in load-voltage total-harmonies distortion level and mean capacitor voltage fluctuation. The method is validated experimentally for this form of MFCI.

## 1 Introduction

The multilevel flying capacitor inverter (MFCI), a relatively new type of power converter topology, has attracted worldwide attention for high power applications such as static power conditioners and large motor drives. Interest stems from the work of Meynard and Foch [1, 2] who applied the basic switched capacitor bridge principle to enable voltage clamping in multiple level power converters. Fig. 1 shows an example of a three-phase four-cell circuit supplying an inductive load. Each phase limb consists of a series of connected cells nested inwardly toward the load from the DC link. Each cell has a capacitor for clamping the node voltage and two bidirectional power switches that operate in a complementary fashion. A greater number of possible output voltage levels requires more cells in each phase limb and a greater total capacitor count. An important advantage of this circuit is that many switch state combinations produce the same voltage level. This gives flexibility in choosing switching control strategies for optimised output performance. It also has a simple arrangement with modular building blocks employing fewer switching devices, and snubberless operation is possible.

Use of MFCIs has been reported for high voltage static VAR compensators [3, 4]. With the flexibility of multiple voltage levels, and if the capacitor voltages are ideally constant, the circuit can regulate the amplitude of the desired sinusoidal voltage by simple staircase control with a very low switching frequency (one state change per switch per cycle) and low harmonic distortion. The well-known selective harmonic elimination (SHE) scheme [5] is often used to determine the electrical angles at which each voltage level is applied. These angles set the fundamental voltage at some specific magnitude and simultaneously suppress certain selected harmonics. For closed-loop operation a look-up table can be established to generate switching angles for different sinusoidal amplitudes desired by the controller. This scheme has been widely applied even for large variable speed drives [6]. Of course, in a practical MFCI, with finite capacitor sizes the voltages across the cell capacitors do vary, but the capacitor values need to be minimised for reasons of size and cost. With low switching frequencies the consequent drawback is in the increased voltage swings on the intermediate voltage levels. This causes excessive voltage stress on the switching devices and the voltage ripple works against low harmonic content in the voltage waveform.

In ensuring proper operation of an MFCI, therefore, the main challenge is to maintain the correct voltage across the floating or cell capacitor. It is essential to appreciate that the MCFI is inherently stable under constant (positive resistance) load conditions. Closed-loop control of capacitor voltages is not fundamentally necessary, because, for a steady load, they automatically settle at a stable fraction of the DC-link voltage. However, closed-loop control can be used to reduce the capacitor voltage swings and to improve response speed at transient load changes. For example, Meynard's group reported a fuzzy logic controller to improve closed-loop capacitor voltage balance [7]. They also developed a voltage observer for use in active cell-capacitor voltage regulation [8, 9]. Other significant work is from the group at Grenoble on a sliding-mode capacitor voltage control (CVC) algorithm [10]. Researchers at Eindhoven investigated capacitor voltage balancing using system modelling [11]. Nearly all these approaches require capacitor voltage measurement, although some resort to mathematical models which are complicated to implement. The concern is that these approaches require a large number of capacitor voltage feedback loops, in addition to the output load voltage measurement. For example the converter of Fig. 1 requires nine additional capacitor voltage feedback loops. This number increases with an increasing number of voltage levels and the control strategy for load voltage/current becomes complicated.



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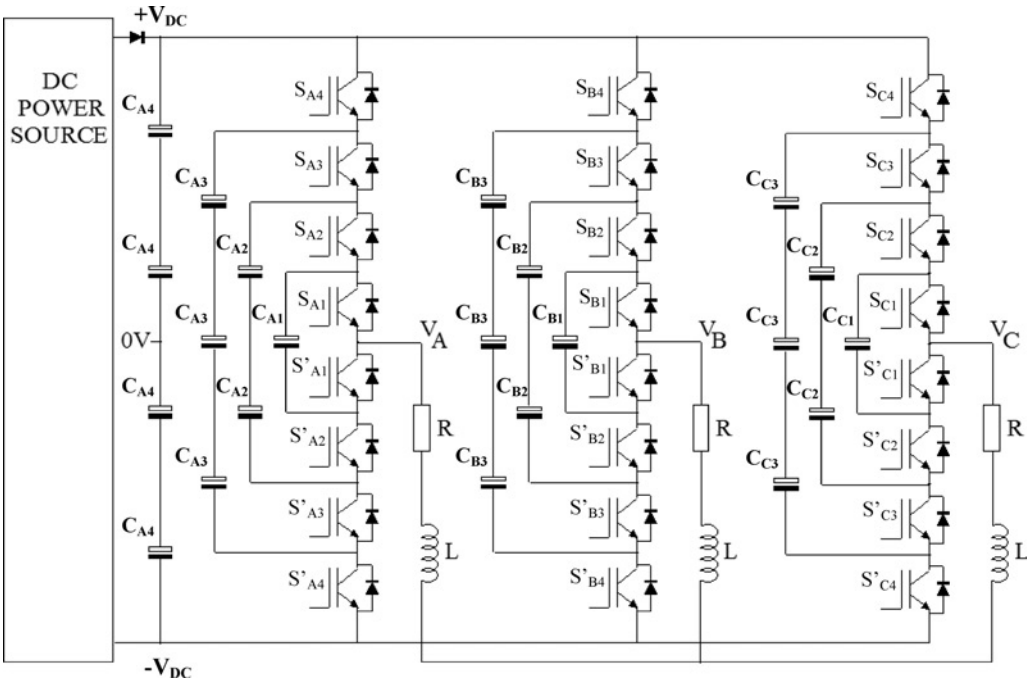


**Fig. 1** *Five-level flying-capacitor inverter circuit*

The present paper investigates a rule-based switching strategy for capacitor voltage balance without cell-capacitor voltage feedback controls. The scheme employs a switching pattern selection mechanism which, not only maintains nil mean current flowing in all capacitors, but also minimises the inevitable fluctuation in the voltage across capacitors of finite value. The scheme is simple compared with the conventional feedback approach. It requires load voltage and current measurements to determine the load power factor and current direction. As these are already available in an inverter system, no additional sensors are required. The method is developed for sinusoidal voltage generation using the SHE technique and devices are switched only at or near fundamental frequency. Though the analysis and simulation studies of the method described here are concentrated on steady-state operation, the method can be used for output voltage feedback control, such as in high–voltage VAR compensators. Experimental results will demonstrate that balanced capacitor voltages are obtained, and hence total harmonic distortion (THD) of output line voltage/current is significantly reduced.

## 2 Switching states and sequences for balancing requirement

### 2.1 Switching states

As shown in Fig. 1, for an $N$-cell flying capacitor inverter, each limb has $2N$ bidirectional switches (IGBT and anti-parallel diode combination) and can provide $N+1$ distinct DC voltage levels from zero to $V_{dc}$, at the load terminal with respect to the negative DC link voltage. When two limbs are configured as a full-bridge inverter it can apply $2N+1$ distinct voltage levels across the load. In a balanced inverter, the floating cell-capacitor average voltages are ideally kept at multiples of $V_{dc}/N$, therefore, the cell-capacitor voltages will range between $V_{dc}/N$ and $(N-1)V_{dc}/N$, with the lowest voltage across the capacitor associated with the complementary switch pair nearest the load terminal.

The number of switching states $M$ capable of producing any particular intermediate voltage level (including zero volts) can be calculated by the formula [12]

$$M_k = \frac{1}{(N-k)!} \times \prod_{n=0}^{N-k-1} (2N-n) \quad \text{for} \quad 0 \le k < N \quad (1)$$

where $k$ defines the level number and is equal to 0 for the 0 V level. Thus, for example, for a two-cell full bridge circuit to generate an output voltage equal to $-V_{dc}/2$, $M_k = 4$. When the number of cells $N = 4$, as in Fig. 1, $M_k = 15$ for an output voltage of $-V_{dc}/4$. This above relationship quantifies the complexity of the operating modes available in flying-capacitor inverters. This increases greatly as the number of levels is increased as is illustrated in Table 1.

### 2.2 Selective harmonic elimination (SHE) scheme

To synthesise a desired sinusoidal waveform, the flexibility of multiple voltage levels allows simple staircase control,

**Table 1: Single-phase full-bridge flying-capacitor inverter switching states**

| Level (N + 1) | Switches | Capacitor cells | Total no. of switch states | Switch modes for 0V |
|---|---|---|---|---|
| 3 | 8 | 2 | 16 | 6 |
| 4 | 12 | 3 | 64 | 20 |
| 5 | 16 | 4 | 254 | 70 |
| 6 | 20 | 5 | 1024 | 252 |

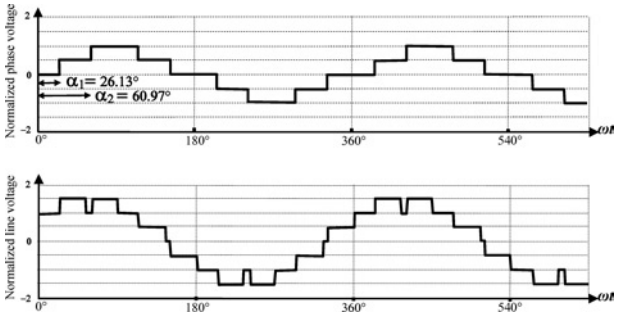


**Fig. 2** *Ideal phase and line voltages, normalised to $V_{dc}$, for SHE control ($m_a = 0.85$)*

whereby each voltage level is applied across the load at predefined electrical angles in a fundamental cycle. Using the selective harmonic elimination (SHE) scheme, the switching angles of the inverter can be determined to set the fundamental voltage at some specific magnitude and simultaneously suppress certain harmonics. In its simplest control form, the resultant waveform for the phase voltage of the inverter in Fig. 1 has the shape of a staircase as shown in Fig. 2. SHE determines each of the switching angles according to the Fourier series expressed as

$$V(\omega t) = \sum_{n=1}^{\infty} b_n * \sin(n * \omega t) \tag{2}$$

where

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\omega t) * \sin(n * \omega t) * \mathrm{d}(\omega t)$$

where the time origin is placed, for convenience, at the zero crossing of the fundamental component. The control scheme maintains the output as an odd function of time, as implied in this Fourier series and as shown in Fig. 2. For the four-cell five-level circuit, only two angles are determined to perform control with the fundamental regulated and one harmonic eliminated. Numerical techniques are applied to solve the nonlinear equations

$$b_1 = \frac{4}{\pi} * V_{DC} * (\cos(\alpha_1) + \cos(\alpha_2)) = m_a \times 2 \times V_{DC} \tag{3}$$

and

$$b_5 = \frac{4}{5 * \pi} * V_{DC} * (\cos(5 * \alpha_1) + \cos(5 * \alpha_2)) = 0 \tag{4}$$

for $\alpha_1$ and $\alpha_2$ which are 26.13° and 60.97°, respectively. Fig. 2 shows the resultant staircase shaped phase and line voltage waveforms when the peak magnitude of the fundamental component is set to 85% of $V_{dc}$.

### 2.3 Switching sequences

It has already been shown that there is more than one switching state capable of providing an intermediate level voltage at the load terminal of the inverter. For ideal cell capacitors with infinite capacitance, choosing the switching state at each voltage level would be relatively simple. However, in a real system, the different switching states at a given voltage level lead to different current paths within the flying-capacitor inverter circuit. The current flowing through the cell-capacitors will cause the voltages to vary and this variation is proportional to the amplitude, polarity and conduction duration of the current. In addition the power devices' switching losses need to be kept as low as possible, for high efficiency, and their level of usage should also balance. Thus, the selection criteria obey the following:

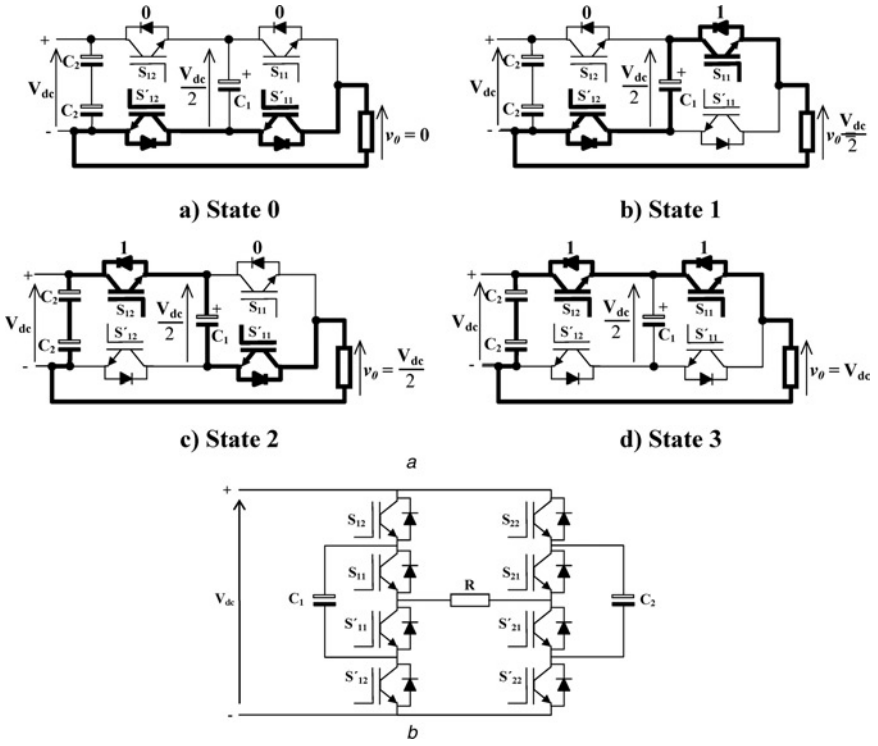


**Fig. 3** *Control of a two-cell three-level flying-capacitor inverter*

*a* Four switching states for a single limb
*b* Full-bridge circuit

(1) allow one independent switch changing state per voltage transition;
(2) maintain capacitor voltage balancing;
(3) maintain equal switch device usage, hence thermal balance.

Items 2 and 3 are related; i.e. achieving capacitor voltage balance ensures the inverter is thermally balanced with all switches having the same average loss.

The flying-capacitor inverter can operate with inherent capacitor voltage balancing so long as the control utilises all the modes of charging and discharging at an intermediate voltage level [1, 2]. This can be illustrated using the simplest case where a two cell three-level inverter supplies a resistive load. Fig. 3*a* shows all the possible switching states, hence current paths, for the inner cell of one limb of such a circuit. States 0 and 3, and states 1 and 2 form, respectively, complementary pairs where their correct usage can ensure balancing of the capacitor voltages and device power loss. In a steady state, states 1 and 2 can be used for equal times within a half cycle, if they are used in turn at the points of rising and of falling voltage. With the resistive load, the load current will be the same at these two instants, so the net change in capacitor charge will be balanced to zero after only one half cycle. Average device losses will also be the same. States 0 and 3 do not affect the capacitor charge, but their complementary usage must ensure that they occur at times where the load current, even if the load is reactive, is of equal and opposite polarity, and this ensures the same average losses in each power device.

Another useful illustration is the two-cell full-bridge inverter shown in Fig. 3*b*. There are four independent switches $S_{12}$, $S_{11}$, $S_{22}$, $S_{21}$ and their combined state can be represented as 4 binary bits in the same order. Initially, a suitable switching state sequence for synthesising the positive half cycle of a sine wave may be [0000] → [0100] → [1100] → [1000] → [0000]. Likewise the switching state sequence for the negative half cycle may be [0000] → [0001]→ [0011]→ [0010]→ [0000]. Even for a partly reactive load, such a sequence, ensures that capacitor voltages are balanced within one complete sinusoidal cycle, as charging and discharging of each of the capacitors takes place at the same voltage and current levels for the same length of time. Meanwhile the total turn-on durations for devices at the same current level but in different limbs are also equal, hence achieving overall thermal balance.

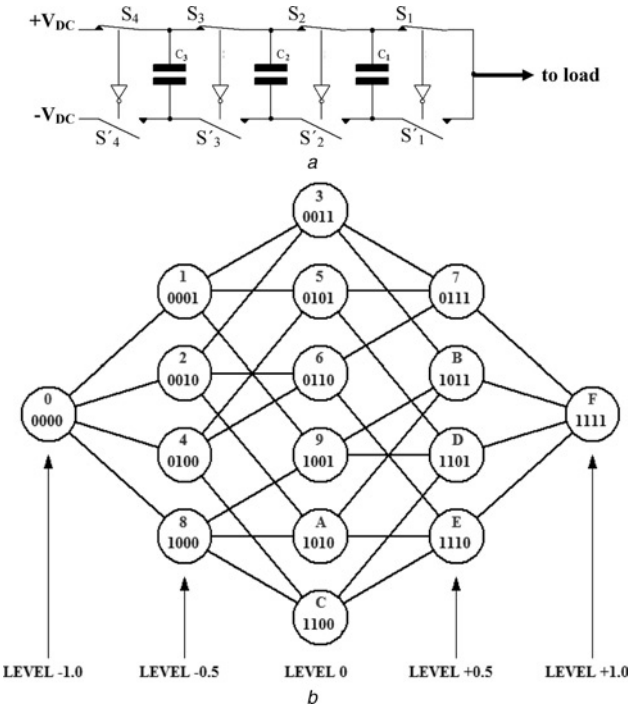


**Fig. 4** *One phase limb of four-cell MFCI of Fig. 1*
*a* Simplified four-cell inverter phase-limb circuit and
*b* its allowable transitions between level states

## 3 Switching pattern selection for *N*-cell inverters

Applying the stated principle, an MFCI with $N$ capacitor cells will require $N$ cycles, hence $N$ switching sequences, to balance the capacitor voltages and equalise the conduction losses in the switches [12]. We refer to a set of $N$

**Table 2: Capacitor voltage net change for each inverter limb switching state**

| Switching state $S_4S_3S_2S_1$ | Output voltage level | Change(+VE)/ discharge(−VE) $C_3$ | Change(+VE)/ discharge(−VE) $C_2$ | Change(+VE)/ discharge(−VE) $C_1$ |
|---|---|---|---|---|
| 0000 (0) | −1.0 | | | |
| 0001 (1) | −0.5 | | | −VE |
| 0010 (2) | −0.5 | | −VE | +VE |
| 0100 (4) | −0.5 | −VE | +VE | |
| 1000 (8) | −0.5 | +VE | | |
| 0011 (3) | 0 | | −VE | |
| 0101 (5) | 0 | −VE | +VE | −VE |
| 0110 (6) | 0 | −VE | | +VE |
| 1001 (9) | 0 | +VE | | −VE |
| 1010 (A) | 0 | +VE | −VE | +VE |
| 1100 (C) | 0 | | +VE | |
| 0111 (7) | +0.5 | −VE | | |
| 1011 (B) | +0.5 | +VE | −VE | |
| 1101 (D) | +0.5 | | −VE | +VE |
| 1110 (E) | +0.5 | | | −VE |
| 1111 (F) | +1.0 | | | |

**Table 3: 24 groups of switching sequences**

| Level 0 | Switching sequence groups | | | |
|---|---|---|---|---|
| 3 + C and 6 + 9 | $\overset{7\ E\ D\ B}{3,6,C,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ 7\ E\ D}{3,6,C,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ 7\ E\ D}{9,3,6,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ B\ 7\ E}{9,3,6,C}$ $\underset{1\ 2\ 4\ 8}{}$ |
| 3 + C and 5 + A | $\overset{7\ B\ D\ E}{3,A,5,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ E\ 7\ D}{3,A,5,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{7\ B\ D\ E}{5,3,C,A}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ 7\ E\ B}{5,3,C,A}$ $\underset{1\ 2\ 4\ 8}{}$ |
| 6 + 9 and 5 + A | $\overset{7\ B\ E\ D}{5,A,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ E\ 7\ B}{5,A,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ 7\ D\ E}{9,6,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ E\ 7\ B}{9,6,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ |
| 3 + C | $\overset{7\ B\ D\ E}{3,3,C,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{7\ B\ E\ D}{3,3,C,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ 7\ D\ E}{3,3,C,C}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ 7\ E\ D}{3,3,C,C}$ $\underset{1\ 2\ 4\ 8}{}$ |
| 5 + A | $\overset{7\ B\ D\ E}{5,A,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{7\ E\ D\ B}{5,A,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ B\ 7\ E}{5,A,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ E\ 7\ B}{5,A,5,A}$ $\underset{1\ 2\ 4\ 8}{}$ |
| 6 + 9 | $\overset{B\ 7\ E\ D}{9,6,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{B\ E\ 7\ D}{9,6,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ 7\ E\ B}{9,6,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ | $\overset{D\ E\ 7\ B}{9,6,6,9}$ $\underset{1\ 2\ 4\ 8}{}$ |

switching sequences as a switching pattern, and the criteria for a good switching pattern are:

- having no switching states which cause a capacitor to be charged and subsequently discharged, or vice versa, at peak current;
- switching states being well matched to ensure nil net charge accumulations in all cell capacitors.

A rule-based selection scheme is now accordingly developed and tested, using a four-cell five-level inverter as an example. The method can be extended to an MFCI of any number of levels.

### 3.1 Switching states and sequences in a four-cell inverter

A simplified diagram for one phase-limb of the four-cell MFCI given in Fig. 1 is shown in Fig. 4*a*. There are 16 distinct switching states for this circuit. Table 2 lists all of them, represented as 16 binary numbers, their corresponding normalised output voltage level and net charging effect, on each of the cell capacitors, for a positive load current. The most significant bit of these binary numbers controls the outer complementary switch pair nearest the DC link ($S_4$). '1' indicates that the upper switch is in conduction and corresponds to a nonzero voltage level at the relevant inverter output terminal. As can be seen in the Table, the switching states for the normalised voltage levels −0.5 and 0.5 all lead to different charging effects in the three cell capacitors, hence causing the voltage swings.

Considering the charging and discharging characteristic for all capacitors in this inverter, the switching states for 0 voltage level can be grouped in three complementary pairs, i.e. states 3 & C, states 5 & A and states 6 & 9, as shown in Table 3.

Synthesising a sinusoidal cycle using the SHE staircase requires the inverter stepping through a set of three intermediate states, i.e. a switching sequence, from voltage levels −1 to +1. The possible switching sequences are limited first by selection condition 1 listed in Section 2, so the number of allowable transitions between switching states in this inverter is as illustrated in Fig. 4*b*. In total there are four possible paths between level −1 and a level −0.5, three between any for level −0.5 and a level 0, two between any for levels 0 and a level +0.5 and one between any level for +0.5 and level +1. Thus, 24 different sequences of switching states can be used when stepping up the nominal voltage level from −1 to +1. For instance, the switching states to be used in one cycle may be 0 [0000], 1 [0001], 9 [1001], D [1101] and F [1111], in hexadecimal notation. This is a switching sequence labelled as $\overset{D}{\underset{1}{9}}$. Adapting this labelling method, the 24 possible switching sequences are listed as follows

$$\overset{7\ B\ 7\ D\ B\ D\ 7\ B\ 7\ E\ B\ E\ 7\ D\ 7\ E\ D\ E\ B\ D\ B\ E\ D\ E}{3,3,5,5,9,9,3,3,6,6,A,A,5,5,6,6,C,C,9,9,A,A,C,C}$$
$$\underset{1\ 1\ 1\ 1\ 1\ 1\ 2\ 2\ 2\ 2\ 2\ 4\ 4\ 4\ 4\ 4\ 8\ 8\ 8\ 8\ 8\ 8}{}$$

### 3.2 Valid switching patterns and their selections

A pattern for a four-cell inverter consists of four switching state sequences for four cycles. To choose the best pattern, it is necessary to investigate the total number of valid patterns for this inverter. Also, in this study, it is assumed that the load is inductive, so the current waveform is sinusoidal and the phase current lags the phase voltage fundamental component.

A good starting point in identifying valid balancing switching patterns is to keep the individual level switching states the same over one complete cycle, thus using one out of the 24 sequences given in Section 3.1. The subsequent three sequences can be chosen according to the three complimentary pairs of level 0 switching states, it is clear that there are groups of 6 pattern permutations made up of just 4 individual sequences, where the sequence order is varied. These groups of sequences are listed in Table 3, with the level 0 contributing states shown as reference. The basic requirement is that all four −0.5 and +0.5 level states are used, but the level 0 states can be taken from either one complementary pair set or two sets out of the six. Thus, there are in fact 24 different groups of switching sequences. By permutation, each has 6 different patterns, so we have a grand total of 144 valid balancing patterns that meet the minimum switching transition criteria. Taking the upper left group in Table 3 as an example, the 6 pattern permutations in this group are as follows

$$\underset{1\ 2\ 4\ 8}{7EDB}\ \underset{1\ 2\ 8\ 4}{7EBD}\ \underset{1\ 4\ 2\ 8}{7DEB}\ \underset{1\ 4\ 8\ 2}{7DBE}\ \underset{1\ 8\ 2\ 4}{7BED}\ \underset{1\ 8\ 4\ 2}{7BDE}$$
$$36C9,\ 369C,\ 3C69,\ 3C96,\ 396C,\ 39C6$$

With such a large number of possible balancing patterns, the two rules stated earlier in this Section have been applied to

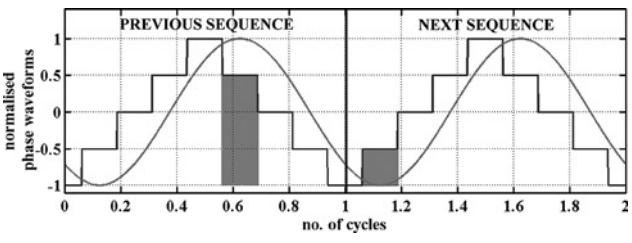


**Fig. 5** *Ideal phase V/I waveforms with 45° lagging current*

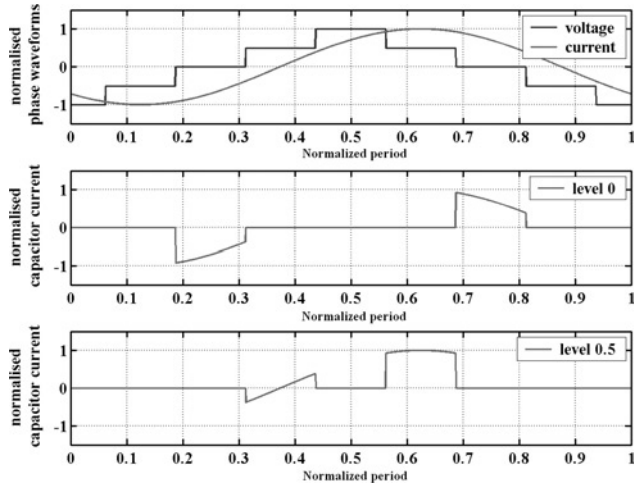


**Fig. 6** *Current flowing through $C_3$ when using switching sequence 4,7,5*

select the best one. The first avoids those switching patterns which cause the same capacitor to be charged and subsequently discharged, or vise versa at peak current. Fig. 5 shows that the phase current magnitudes are peaked at levels +0.5 and −0.5, respectively. Hence, these regions will have the largest levels of capacitor voltage variation. So, if state 7[0111] is used at +0.5 level in the first sequence, the voltage drop on $C_3$ would be the maximum due to the peak current discharging. Subsequently, if applying state 8[1000] at −0.5 level in the immediate sequence, $C_3$ would be charged with the most negative current causing its voltage to reduce further. Thus, the preferred switching state at level −0.5 should not cause the voltage across $C_3$ to change in the same direction as that due to the previous sequence at level +0.5. This can be obtained by excluding the next level −0.5 state being the 1's complement of the previous level +0.5 state. For instance, state 8 [1000] should not follow state 7 [0111]. According to this rule the following consecutive sequences pairs are not preferred

$$\begin{matrix} 7 & Y \\ X & X \\ Z & 8 \end{matrix}, \begin{matrix} E & Y \\ X & X \\ Z & 1 \end{matrix}, \begin{matrix} D & Y \\ X & X \\ Z & 2 \end{matrix} \text{ and } \begin{matrix} B & Y \\ X & X \\ Z & 4 \end{matrix}$$

In this notation, symbols *X*, *Y*, *Z* indicate indifferent states which need not be the same in consecutive columns.

The second rule considers the charging/discharging of capacitors within one sinusoidal cycle due to the switching sequence used. The aim is to ensure that a particular capacitor is in the same current path over this cycle, so that the capacitor concerned has no, or as little as possible, net charge accumulation. As shown in Table 2, when adjacent switches are in the opposite state, the capacitor between them lies in the load current path, and so its voltage would swing. Again, with regard to the peak and trough of the current occurring around level +0.5 and level −0.5, respectively, it is preferable if as many cells as possible are in the same state at both levels. Priority for this rule can be assigned to the higher voltage capacitor, i.e. $C_3$, as it will see the largest voltage change. For example, if at level −0.5 the switching state is 4 [0100], then state 7 [0111] is preferred for level +0.5. In both sequences, $C_3$ lies in the load current path and is in discharging mode. Fig. 6. shows the resultant current flowing through $C_3$. As can be seen, there is symmetry in the cell-capacitor current, and so the mean current is zero leading to no net change in cell-capacitor voltage. Applying the same rule, states 8 [1000] and B [1011] are also preferred within a sequence as $C_3$ is in charging mode for both voltage stepping-up and down cases. As only one pair of switching devices is allowed to change state at a time, only four sequences would be preferred for minimising the voltage variation on $C_3$ over

**Table 4: Comparison between two switching patterns and ideal case**

| Parameter | Switching patterns | | | | |
|---|---|---|---|---|---|
| | Ideal | Pattern 1 | | Pattern 2 | |
| Actual modulation depth, $m_a$ | 1.000 | 1.029 | | 1.030 | |
| Power factor | 0.694 | 0.697 | | 0.686 | |
| Phase voltage THD, % | 19.25 | 16.92 | | 23.81 | |
| Line voltage THD, % | 14.53 | 13.07 | | 19.88 | |
| Phase current THD, % | 1.76 | 3.49 | | 9.41 | |
| | Ideal voltage | Actual voltage | %Voltage ripple | Actual voltage | %Voltage ripple |
| Capacitor mean voltages (% of unit cell voltage) | 100.0 | 98.0 | 2 | 75.7 | 24.3 |
| | 200.0 | 198.4 | 1 | 197.5 | 1.25 |
| | 300.0 | 312.1 | 4 | 333.2 | 11 |
| | 400.0 | 400.0 | 0 | 401.9 | 0.47 |
| Mean ripple voltage, % | | | 1.75 | | 9.255 |
| Capacitor peak voltages (% of unit cell voltage) | 100.0 | 110.4 | 10.4 | 105.1 | 5.1 |
| | 200.0 | 212.1 | 6.05 | 240.5 | 20.1 |
| | 300.0 | 322.3 | 7.38 | 376.3 | 25.1 |
| | 400.0 | 418.2 | 4.55 | 431.0 | 7.75 |
| Mean peak voltage, % | | | 7.1 | | 14.5 |
| Switch peak blocking voltages (% of unit cell voltage) | 100.0 | 110.4 | | 105.1 | |
| | 100.0 | 128.6 | | 170.1 | |
| | 100.0 | 167.8 | | 205.9 | |
| | 100.0 | 137.2 | | 140.3 | |

one sequence cycle, and, in each case, $C_3$ is in the same current path throughout the cycle. These are

$$\overset{7}{5},\overset{7}{6},\overset{B}{9} \text{ and } \overset{B}{A}$$
$$4\quad 4\quad 8\qquad 8$$

According to this rule there are 4 sequences, shown as follows, preferred within a pattern

$$\overset{7}{5},\overset{7}{6},\overset{B}{9} \text{ and } \overset{B}{A}$$
$$4\quad 4\quad 8\qquad 8$$

When applying this second rule to $C_2$, and to $C_1$, states in the adjacent cells around $C_3$ must not be complements, otherwise this rule will be broken, therefore this means that the following 4 sequences are preferred for use in a pattern:

$$\overset{D}{5},\overset{D}{C},\overset{E}{6} \text{ and } \overset{E}{A}$$
$$4\quad 4\quad 2\qquad 2$$

Applying the preceding two rules, one particular pattern out of 144 is judged to offer the best performance, namely

$$\overset{7EDB}{36C9} \qquad \text{(Pattern 1)}$$
$$1248$$

This pattern does not have any consecutive states which break the first rule governing the level +0.5 followed by level −0.5. It also contains 2 sequences from the second rule which have preferred state combinations for levels −0.5 and +0.5.

The various balancing patterns have been screened for ones which are likely to cause poor overall performance. One such pattern, which breaks the first rule only, has one good sequence from the second rule for $C_1$ and is as follows

$$\overset{7BED}{3AC5} \qquad \text{(Pattern 2)}$$
$$2841$$

The same rule-based analysis can be done for other load characteristics. In the case of a leading phase current angle, the second rule governing a sequence still applies; the first rule's reasoning is the same but applied this time to a sequence level −0.5 state followed by the next sequence level +0.5 state.

The overall pattern, thus derived, is repeated once every four cycles (number of cells), with different switch states used at the same voltage level of each cycle.

## 4 Comparison of balanced switching patterns

To confirm that the rules governing the pattern selection are valid, simulation studies of all the preceding-listed 144 switching patterns were carried out [13], but, to save space, only results for switching patterns 1 and 2 identified in Section 3 are presented in Table 4. These are also compared with the ideal case when constant capacitor voltages are always maintained. The performance criteria for the best pattern are the minimum THD values, for both load voltage and current, and lowest percentage capacitor voltage variations. In simulation the DC link voltage was set to 400 V and control settings were $m_a = 1$ and a fundamental frequency of 50 Hz, using 5th harmonic elimination angles for staircase SHE control. The phase voltage fundamental is therefore 141.4 V(RMS) and the line voltage fundamental is 244.9 V (RMS). The load model used has component values R = 2.5 Ω and L = 7.958 mH, and the individual cell capacitance is 10 mF. The nominal output power for an

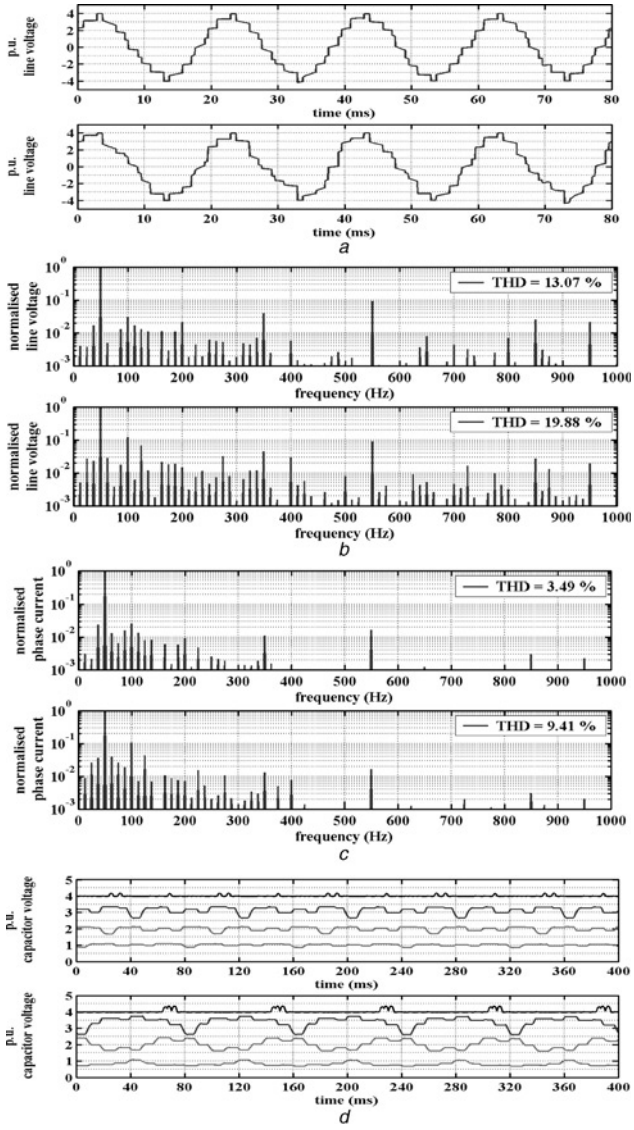


**Fig. 7** *Comparison of two switching patterns; PATTERN 1 (upper), PATTERN 2 (lower)*

*a* Line voltage waveforms
*b* Line voltage spectra
*c* Load phase current spectra
*d* Capacitor voltages

**Fig. 8** *Experimental four-cell five-level flying-capacitor inverter assembly*

equivalent ideal sinusoidal system is 12 kW with power factor 0.707.

The results obtained, as can be seen in Table 4, confirm our prediction; Pattern 1, $\begin{pmatrix} 7\,E\,D\,B \\ 3\,6\,C\,9 \\ 1\,2\,4\,8 \end{pmatrix}$, offers lower output waveform harmonic distortion compared to Pattern 2, $\begin{pmatrix} 7\,B\,E\,D \\ 3\,A\,C\,5 \\ 2\,8\,4\,1 \end{pmatrix}$, with THD values for phase voltage being 16.92% against 23.81%, and for line-line voltage 13.07% against 19.88% . Its phase and line voltage THDs are even lower than the ideal case. The phase current THD is also significantly lower than that resulting from Pattern 2. Figs. 7*a* and *b* show the line voltage waveforms and their spectra for the two cases, with the frequency components normalised to the fundamental. Clearly, Pattern 1 gives better waveform with lower THD level than its counterpart. Notice that a 12.5 Hz component is present in the voltage spectrum for both patterns, and its magnitude is higher for the inferior Pattern 2. This component is due to the balancing pattern control strategy which repeats every four cycles, i.e. 12.5 Hz. Phase current spectra for both patterns are shown in Fig. 7*c*.

The capacitor voltage waveforms, shown in Fig. 7*d*, are the most revealing. The individual cell-capacitor voltages (plotted on the same zero axis for reference) of the inverter controlled by the two balancing pattern schemes are shown. As listed in Table 4 with Pattern 1, voltage ripple is reasonably low with mean ripple voltage only 1.75%, whereas Pattern 2 is significantly higher at 9.25%. The mean peak voltage variance for Pattern 1 is also lower than Pattern 2 at 7.1% to 14.5%. The peak blocking voltage for Pattern 1 is at $\pm 50$ % of the nominal values, but, for Pattern 2, it is significantly higher at around 100% of the nominal level. This is the primary reason for Pattern 2's poorer waveform performance.

It should be stressed that this proposed method, though it does not require capacitor voltage measurements, needs to have information on load current direction, magnitude and phase angle. These are usually available in a converter system. Like the SHE scheme, the method will suit particularly well to high power applications with low switching frequency and dynamics. In particular, it can be applied in combination with SHE, for closed-loop regulation of the terminal voltage of a static VAR compensator with constant frequency. Switching angles for different

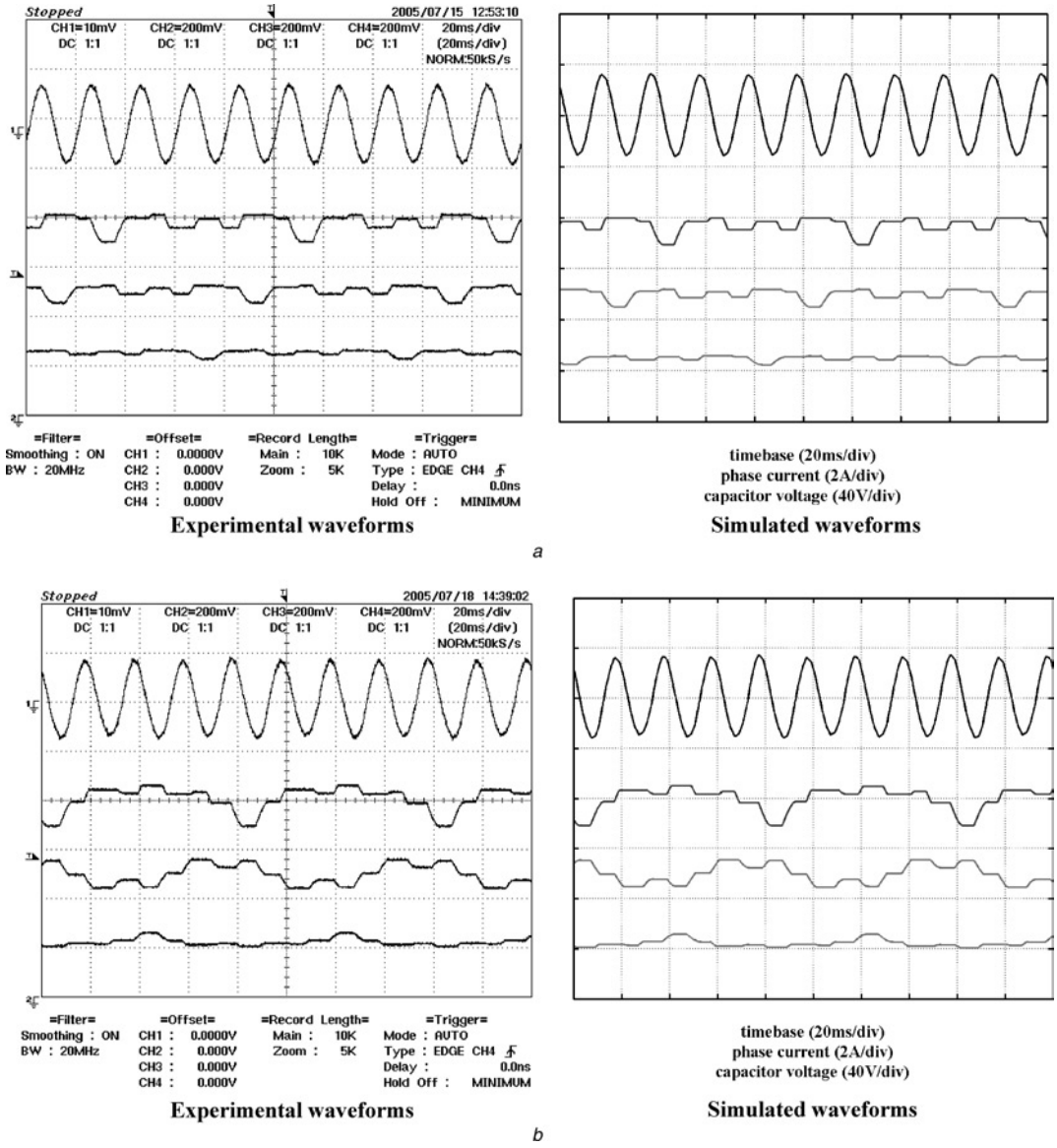


**Fig. 9** *Comparison of experimental and simulation results*

*a* Phase current and cell capacitor voltages for PATTERN 1
*b* Phase current and cell capacitor voltages for PATTERN 2

sinusoidal magnitudes can be calculated off-line and stored in a ROM. The switching sequences and charging/discharging patterns for each capacitor during previous cycles need to be stored and updated every $N$ cycles. Suitable switching sequences can be selected according to the present instantaneous current direction and magnitude.

## 5 Test of a four-cell laboratory prototype inverter

This rule-based method has been tested on a practical four-cell MFCI. As a design starting point, 5% current harmonic distortion is acceptable. The maximum load power is assumed to be about 1.0 kW with a lagging power factor of around 0.7. The DC link voltage is 400 V, so the unit cell voltage is 100 V, the required capacitance has to be greater than 1.02 mF to avoid excessive voltages across the switches. For the practical inverter, standard-value 1 mF electrolytic capacitors, with a peak voltage capability of 200 V, have been used. The power switches need to cope with a peak voltage of at least 150 V. The IRG4PC30KD 30 A 600 V IGBT (International Rectifier), incorporating an antiparallel diode of equivalent rating, is appropriate.

The assembled inverter is shown in Fig. 8, with the cell capacitors clearly visible below each set of inverter PCBs. There is also one 1 mF 450 V electrolytic capacitor across the DC link connections to the inverter.

The digital gate firing pulse generation and the different forms of control scheme are implemented on a Memec Spartan-II$^{TM}$ LC development board. This is a low-cost evaluation platform based around a 100 k gate Xilinx Spartan-II Field Programmable Gate Array (FPGA). Control schemes written in VHDL are described by Watkins [13].

To confirm the predictions of optimum balancing pattern selection for SHE control, the load was set to give a power factor of 0.6 by setting the load resistances to 37.5 Ω with 160 mH inductors. The inverter was then operated with pattern $\overset{7\,E\,D\,B}{\underset{1\,2\,4\,8}{36C9}}$ (Pattern 1) and pattern $\overset{7\,B\,E\,D}{\underset{2\,8\,4\,1}{3AC5}}$ (Pattern 2), and the various operating parameters were measured.

Figs. 9*a* and *b* show the measured cell-capacitor voltage waveforms for two different balancing control patterns, with the phase current shown for reference. The simulated waveforms are also included in the Figures for comparison. As can be observed, the practical waveforms resemble very well to their corresponding simulated ones. This fact validates our earlier predicted performance. Pattern 1 control exhibits a lower peak-to-peak voltage ripple than the Pattern 2 case. The repetition frequency of the cell-capacitor voltages is 12.5 Hz, in both cases, due to the balancing patterns. There is a marked difference in the harmonic content of the line voltage between the two operating patterns, as can be seen in the spectra plots of Fig. 10. These show that Pattern 1 offers superior performance compared with that given by Pattern 2, with lower unwanted harmonics. The computed THD and spectral signature of the measured voltages show good agreement with those predicted by simulation in both cases. Pattern 1 was in fact shown to be the rigorous optimum when all 144 patterns were compared [13], and Pattern 2 was chosen here as just one example of many inferior ones.

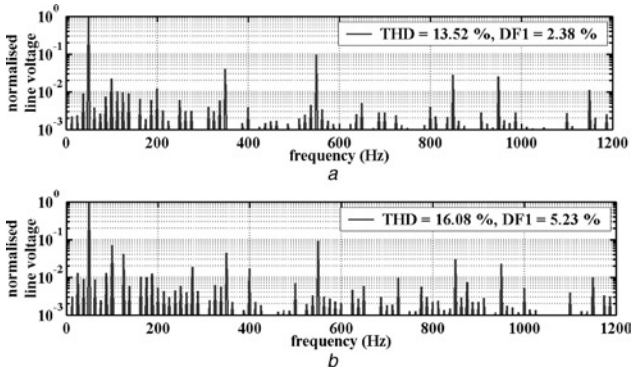


**Fig. 10** *Comparison of experimental results*

*a* Line voltage spectra for PATTERN 1
*b* Line voltage spectra for PATTERN 2

## 6 Conclusions

Capacitor voltage swings degrade the output voltage performance of an MFCI. The paper presented a rule-based capacitor voltage balancing strategy working with the selective harmonic elimination scheme for load voltage performance. The method does not require capacitor voltage measurement but only a load current sensor. Switching states for a three-phase four-level flying capacitor inverter were investigated. Criteria were identified to choose the switching sequence/patterns which would cause least disturbances to the capacitor voltages. The algorithm was developed and validated experimentally in the open-loop case, but it can be applied effectively for closed-loop control of the load terminal voltage, without the complexity of using individual capacitor voltage feedback.

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