Analysis and Control of A Multi-level Flying Capacitor Inverter

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Abstract - The paper presents the results of a study into the optimal switch mode sequence for a multi-level flying capacitor inverter to synthesis a sinewave voltage under staircase angle control. It is shown that a properly selected sequence will yield the voltage and loss balances in capacitor voltages and switching devices respectively and minimize the load voltage THD values. A general mathematical model for an N-level inverter is presented which can be conveniently applied for computer simulation of any operating mode.

I. INTRODUCTION

Multilevel inverters are a type of power converter topologies aimed at high power applications such as traction motor drives and static power conditioning systems. In a multilevel inverter, an increased number of power switches are configured to provide several levels of voltage to the load. The inverter can then be controlled in a simple manner to synthesize an approximated sinusoid from the available voltage level states.

There are several benefits of multilevel inverters compared with present two-level pulsewidth modulation inverters. These circuits allow existing power switches to be used in systems where voltages higher than the individual switch rating are applied to the load. The switching losses in the power converters are reduced because of the increased flexibility for voltage waveform synthesis offered by the increased number of voltage levels. In addition, as the harmonic distortion of the output wave is much decreased less filtering is required. For applications in adjustable speed drives, the voltage stress across the motor winding is reduced due to lower voltage change rates(*dV/dt*).

There are three main types of multilevel inverter topology [1,2]:

- Diode-clamped
- Flying-capacitor
- Cascade-bridge

The diode-clamped circuit imposes restrictions on the allowed switching modes and requires a carefully designed control strategy for capacitor voltage balancing. The cascade-bridge has the problem of using separate isolated multiple DC power supplies and hence can be expensive.

The flying-capacitor voltage source multilevel inverter uses capacitors to clamp the voltages of the power switch chain nodes. The three-level implementation of this circuit is shown in Figure 1. An important advantage of this circuit lies in having multiple switching combinations for the same voltage level. This gives flexibility in switching control strategies to achieve optimized output performance. The topology was first disclosed in the early 1990s by Meynard and Foch [3, 4, 5]. The power switches are operated as complementary pairs, and intermediate voltage levels are realized by routing the load current through paths that include the clamping of cell capacitors.

This paper presents a system level study of the flying-capacitor multilevel inverter using computer simulation. Taking a three-level circuit as an example, a systematic method for switching mode analysis is described. A mathematical model for a general N-level flying–capacitor inverter is given. Finally a switching sequence which is optimal for obtaining both capacitor voltage and switch duty cycle balancing and satisfying the required harmonic performance is presented.

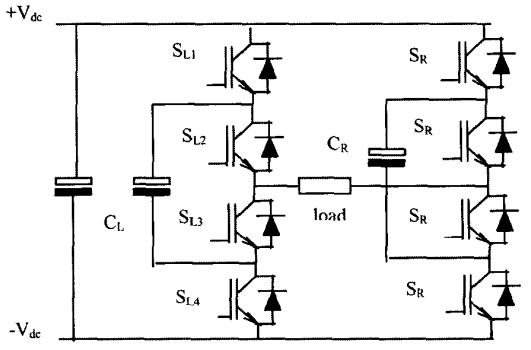


Figure 1 Three-Level Flying-Capacitor Inverter

II. OPERATING FEATURES

The flying-capacitor inverter can theoretically be constructed to give an unlimited number of voltage levels, but practical designs are usually limited to six levels. The number of possible voltage levels is related to the number of power switching devices connected in series in each inverter leg. The circuit inverter leg is in the form of a series of connected cells nested inwardly toward the load from the dc-link. Each cell has a capacitor and two bi-directional power switches operated in a complementary fashion. In an N-cell inverter each limb has 2N switches and applies N+1 distinct dc voltage levels from zero to V_{dc} across the load. The single-phase full-bridge inverter can also apply negative voltage levels across the load and so an N-cell inverter has 2N+1 distinct voltage levels.

The operation modes of a flying–capacitor single-phase bridge inverter need to be analysed systematically as the circuit is complex and the degree of complexity increses with the number of voltage levels. It is important to note that a valid operation mode for a flying–capacitor voltage source inverter must satisfy the following conditions; namely

- it does not cause short-circuiting of the input voltage source/capacitors, and
- it defines the output voltage of the inverter in a finite level.

The analysis can be illustrated by using a two-cell, three-level inverter as an example. As shown in Figure 1, there are eight switching device and anti-parallel diode pairs in the circuit. To satisfy condition 1 the switches in each leg are controlled in complementary pairs, i.e.

$$S_{L1} = \overline{S}_{L4},\ S_{L2} = \overline{S}_{L3}, S_{R1} = \overline{S}_{R4}, S_{R2} = \overline{S}_{R3}$$

where S_L and S_R represent the left and right half-leg switch states, respectively. Thus there are only four independent switches. Setting 1 for when a switch is ON and 0 for when it is OFF, there are sixteen valid switching modes producing five distinct voltage levels. Fig. 2 lists all these switching states and their corresponding voltages with associated current paths highlighted. As can be seen, there is more than one switching mode capable of synthesizing the half DC voltage level (4 for $+V_{DC}/2$ and 4 for $-V_{DC}/2$). These intermediate voltage levels are associated with either charging or discharging the cell-capacitors. In order to maintain charge equilibrium on the capacitors in continuous operation, a switching sequence must be arranged by adequate selection of the switching states. This will be discussed in the next section.

Extending the above analysis to an N-cell inverter, the number of switching modes, *M*, capable of producing any particular voltage level can be calculated by the formula

$$M_k = \frac{1}{(N-k)!} \times \prod_{n=0}^{N-k-1}(2N-n) \text{ for } 0 \le k < N \qquad (1)$$

where k defines the level number and equals 0 for the 0V level and N for the maximum voltage level in an N-cell inverter, thus

$$M_k = 1 \text{ for } k = N \qquad (2)$$

The above relationships are useful in quantifying the complexity of the operating modes available in flying-capacitor inverters. This complexity increases greatly as the number of levels is increased and is illustrated by the different level inverter characteristics in Table 1.

TABLE I
Flying-Capacitor Inverter Complexity

Level	Switches	Capacitor cells	Total States	0V States
3	8	2	16	6
4	12	4	64	20
5	16	6	256	70
6	20	8	1024	252

III. OPTIMAL SINEWAVE GENERATIONS

To synthesize a desired sinusoidal waveform the flexibility of multiple voltage levels allows simple staircase control whereby each voltage level is applied across the load at predefined electrical angles in a fundamental cycle. The power quality of the output voltage is an important criterion in selecting the control angles. This is defined, in general, by the level of total harmonic distortion (THD) whilst achieving the desired fundamental amplitude. In addition, for three-phase ac drives the suppression of low order harmonics are often required. The three-phase inverter gives line-line voltage triplen harmonic cancellation, so elimination of the low order harmonics (the 5^{th} , 7^{th} , 11^{th} ..., depending on the number of levels) in the single-phase waveform is important. Thus for a three-level flying-capacitor inverter, if the required amplitude modulation index is 0.9 and the DC-link voltage is 312 V, the angles chosen are θ_1= 0.3056rad., θ_2= 0.7514rad., θ_3= 1.1194rad.

It is worth noting that staircase angle control using all the available voltage levels is limited to generating high fundamental amplitude[6]. If the required voltage level is low, then the higher voltage levels are not used and the computation of angles is performed on the equivalent of a lower order level inverter. Alternative schemes using a castlelated waveform have been shown to provide low harmonic distortion levels for low fundamental amplitude.

Having obtained the switching angles the control must decide on the switching state to be selected at each voltage level since for a flying-capacitor inverter there are more than one switching modes available for the same voltage level. The selection should obey the following three conditions; namely,:

- allow one independent switch changing state per voltage transition,
- maintain capacitor voltage balancing, and
- maintain equal switch device usage

The first condition above is to keep the power device switching losses in the system to a minimum in order to maintain the highest system efficiency. In large inverters the loss associated with a power switch transition is significant and so the number of power switches being turned on or off in a cycle needs to be minimized. Therefore only one pair of switches are allowed to commutate at every voltage level change.

The second condition above takes into account capacitor voltage balancing and the third ensures equal device power sharing. Capacitor voltage drift from a predefined restricted band leads to individual power switches operating above their rated voltage blocking limit and can be dangerous. The flying-capacitor inverter can operate with inherent capacitor voltage balancing, so long as the control utilizes all the modes of charging and discharging at an intermediate voltage level [7, 8]. Figure 3 shows all the possible current paths for a one cell-capacitor.

The paths 0 and 3, and the paths 1 and 2 form complementary pairs where their correct usage can ensure balancing of the capacitor voltages and device power loss. In the steady state, paths 1 and 2 can be used over consecutive cycles. As long as their operating period coincides with the same angular position in a cycle the net current to the capacitor will be zero and and device losses are the same. In the case of paths 0 and 3, their complementary usage must entail the same angular periods where the current is of equal and opposite polarity, ensuring the same losses in each power device. Thus for a two-cell inverter, if the four independent switches are in OFF state initially, a suitable switching state sequence for synthesizing the positive half-cycle of a sinewave may be [0000]→[1100]→[1000]→[0000] as shown in Figure 4.

This yields turning S_1 on at θ_1 to raise the output voltage from zero to ½ V_{DC} by discharging capacitor C_1. At θ_2 rad. S_2 is switched on to supply the load directly from the DC power source. During the second quarter of the waveform, at $(\pi-\theta_2)$rad. S_3 is switched on to generate ½ V_{DC} while C_1 is recharged. At $(\pi-\theta_1)$rad. S_3 is turned on for bringing load voltage down to zero. Likewise the switching state sequence for the negative half-quarter may be [0000] → [0001]→ [0011]→ [0010]→ [0000]. It can be seen that the capacitor voltages are balanced within a complete sinusoidal cycle as charging and discharging of each of them takes place at the same voltage levels for the same length of time. Meanwhile the turn-on duration for devices at the same voltage level but different legs are also equal. If the initial switching state is different from the above the switch sequence satisfying the above stated requirements will be different.

For inverters with more than two capacitor cells, selecting switching sequences for synthesizing a sinewave is more complicated. For example, for a three-cell, four-level circuit, the available switch combinations for one half-limb to synthesize a sinewave, when the other half-limb is shorted to the negative DC link, are listed in Table 2. As can be seen, there are, respectively, three switching states giving 1/3rd and 2/3rd intermediary voltage levels. Each state has a different charging/discharging effect on the two cell capacitors. Thus if a switch mode sequence, given as that listed in the cycle 1 section of the Table 3, is applied to generate the first half-cycle of a sinewave, the need to balance the capacitor voltages entails the switch mode sequences for the positive half of the second and third cycles be these listed respectively in Table 3. This ensures that equal charging and discharging of two capacitors are achieved through the use of different modes over the same angular period in different cycles. Thus an inverter with more than two cells (three levels) needs more than one possible series of sinusoid switching sequences that can achieve balancing. It will take N (N=No of cells) cycles to balance the capacitor voltages and equalize the conduction losses in the switches.

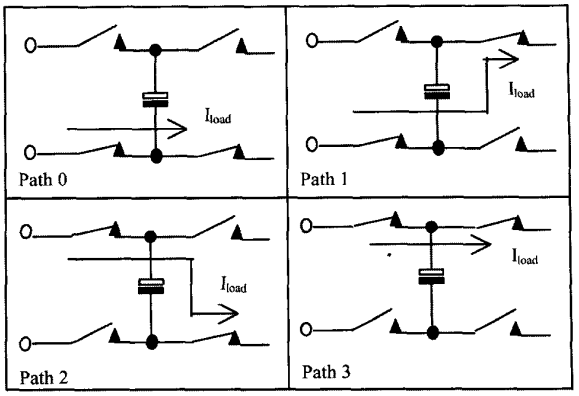


Figure 3: Cell-Capacitor Current Paths

TABLE 2
Switch-modes for a Four-Level Flying-Capacitor Inverter

S_3	S_2	S_1	Output Voltage	C_2	C_1
OFF	OFF	OFF	0V		
OFF	OFF	ON	1/3 V_{DC}		-
OFF	ON	OFF	1/3 V_{DC}	-	+
OFF	ON	ON	2/3 V_{DC}	-	
ON	OFF	OFF	1/3 V_{DC}	+	
ON	OFF	ON	2/3 V_{DC}	+	-
ON	ON	OFF	2/3 V_{DC}		+
ON	ON	ON	V_{DC}		

IV. CIRCUIT MATHEMATICAL MODEL

The fundamental operation and characteristics of the flying-capacitor inverter can offer a great deal of flexibility in terms of operating modes compared with conventional two-level bridges. Complexity increases dramatically as the number of levels increases and this makes it difficult to analyze the circuit operation. Therefore, a simple mathematical model is developed here which can assist circuit analysis under different switch states.

The mathematical equations for the inverter are constructed to express the rate of change of cell capacitor voltage, the output load voltage and the current for all valid switching states. For example for a two-cell, three-level circuit the rate change of capacitor voltage during charging/discharging is given as

$$\frac{dV_{C1}}{dt} = \pm \frac{1}{C_1} i_0 \qquad (3)$$

and the load voltage

$V_O = V_{C1}$ or $V_{DC} - V_{C1}$

for discharging and charging , respectively.

Applying the same principle to any N-cell inverter, the matrix form of the model for a generalized inverter half-leg (chopper) with an R-L load, shown in Figure 4, is as given below:

$$\frac{d[V]}{dt} = -[C]\times[A]^T \times[S]\times i_0 \quad (4)$$

$$v_o = \left[[S]^T \times[A]\right]\times[V] \quad (5)$$

$$\frac{di_o}{dt} = \frac{1}{L}(v_o - Ri_o) \quad (6)$$

where,

$$V = \begin{bmatrix} v_{C_n} \\ v_{C_{n-1}} \\ \dots \\ v_{C_2} \\ v_{C_1} \end{bmatrix}, \; S = \begin{bmatrix} S_n \\ S_{n-1} \\ \dots \\ S_2 \\ S_1 \end{bmatrix},$$

$$A = \begin{bmatrix} 1 & -1 & 0 & 0 & \dots \\ 0 & 1 & -1 & \dots & 0 \\ 0 & 0 & \dots & -1 & 0 \\ 0 & \dots & 0 & 1 & -1 \\ \dots & 0 & 0 & 0 & 1 \end{bmatrix},$$

$$C = \begin{bmatrix} 1/C_n & 0 & 0 & 0 & \dots \\ 0 & 1/C_{n-1} & 0 & \dots & 0 \\ 0 & 0 & \dots & 0 & 0 \\ 0 & \dots & 0 & 1/C_2 & 0 \\ \dots & 0 & 0 & 0 & 1/C_1 \end{bmatrix}$$

and, V is the individual cell capacitor voltage vector and $v_{C_n} = V_{DC}$. Term S is the mode switch state vector where 1 indicates the high-side switch conducting and 0 the low-side switch conducting for each cell complementary pair. Equation (4) represents the load characteristic and may be modified to represent other types of load.

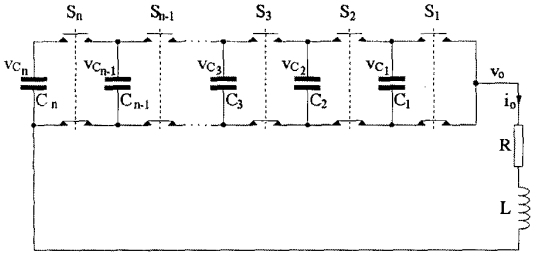


Figure 4: N-level Flying Capacitor Chopper

The above matrix relationships governing the flying-capacitor inverter can be incorporated within a simple fixed time-stepping procedure to calculate the load voltage v_o and current i_o with a particular switch state operated over a specific time period. By combining different switch states operated over different time-periods any switching sequence pattern can be simulated efficiently. This feature is very useful for analyzing inverter operation when synthesizing a sinusoid using a fixed control switching sequence. For example in a three-cell, single-phase inverter the A and C matrices are as follows:

$$A = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \quad \text{and} \quad C = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 2/C_c & 0 \\ 0 & 0 & 1/C_c \end{bmatrix}$$

where C_c is the basic cell capacitance.

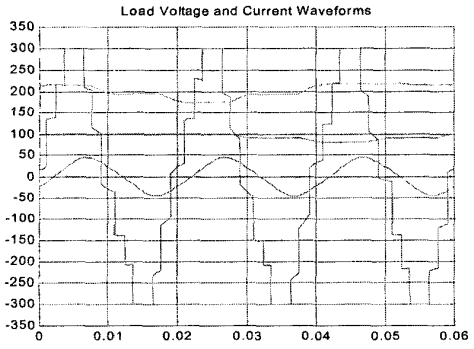
Solving equations (1), (2) and (3) by iteration, the complete output load waveforms can be found for a given switching mode as defined by S.

A series of modelling runs were conducted with all the possible bipolar sequences that give balanced inverter operation in terms of the criteria listed in Section 3. There are 72 possible permutations that satisfy these conditions. Each produces an output voltage waveform with a different THD characteristic. Whilst the one giving lowest THD is naturally preferred, the control must ensure that the voltages across the cell-capacitors are constrained within the range defined by the device blocking voltage rating. Simulation studies on all 72 switching patterns were carried out to analyze these issues and one of these is presented in section IV below.

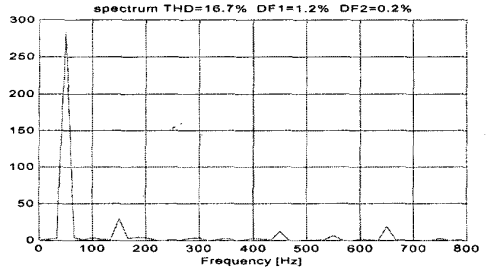
V. Simulation Results

A load of 5 Ω and 13.7 mH in series was used in the simulation to represent a 5.5 kW induction motor phase and the 50 Hz inverter dc-link voltage was set to 300 V. The load waveforms and cell-capacitor voltages are shown in Figure 5(a) with an individual cell-capacitor of 10000 μF for a low THD characteristic. The waveforms are displayed over three cycles to illustrate the inherent capacitor voltage balancing of the switching state sequence used. Figure 5(b) displays the spectrum of the load voltage waveform. There are 'sub-harmonics' at multiples of a 1/3rd of the fundamental since the waveform repeats itself every three cycles; and these are included in the THD calculation.

The example load waveforms were produced for one particular switching state sequence that has a fairly constant THD characteristic irrespective of cell-capacitance. There is a spread of characteristics for the different switching patterns, with some not exhibiting a constant characteristic. Certain patterns cause an increase in the harmonics of the waveform as the capacitance increases and cause an opposite effect.



(a) Load Waveforms



(b) Load Voltage Spectrum

Figure 5: Staircase Control Output Waveforms

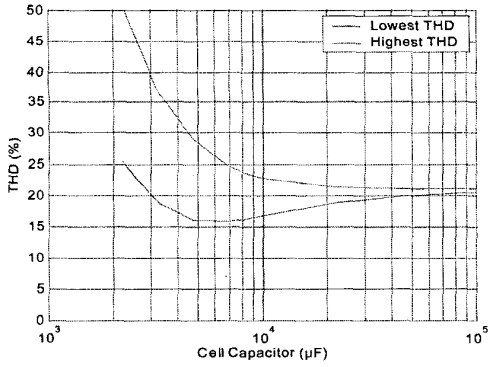


Figure 6: Switching Pattern THD Variation With Cell-Capacitance

Figure 6 illustrates the variation in THD with cell-capacitance for two operating switching state sequences. The two curves represent the switching patterns for boundaries lowest and highest THD characteristic. This clearly indicates that the selection of switching state sequence can have a significant effect of output voltage quality. Optimal control should entail the use of the lower THD value switching pattern

VI. CONCLUSIONS

The paper has investigated the available operating modes for a flying-capacitor form of multilevel inverter. The optimum switch sequence for a four-level inverter synthesizing a sinewave signal has been deduced. The criteria used incorporate the lowest number of switching transitions, equal device usage and capacitor voltage balance. A matrix model capable of expressing all modes of operation of the circuit is presented.

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TABLE 3: Three -Cycle Switch Sequence for a Balanced Operation

	Cycle 1							Cycle 2							Cycle 3							
S_1	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1	0
S_2	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0
S_3	0	0	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0
C_1		-	-		+	+			-			-				+			+		0
C_2			+			-				-		+	+			-	-			+	

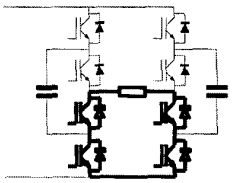
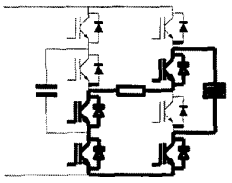
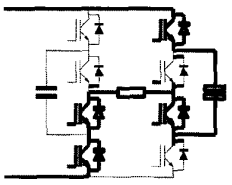
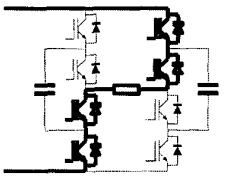
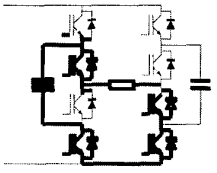
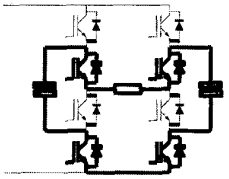
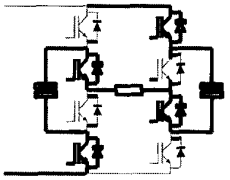
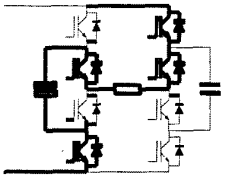
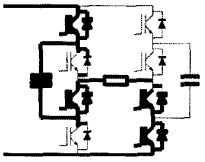
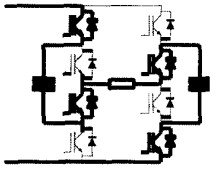
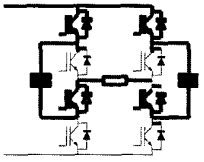
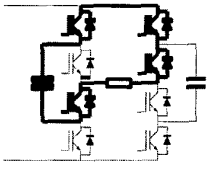
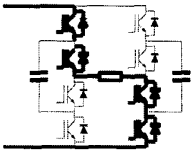
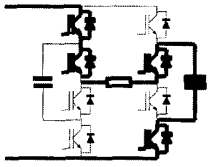
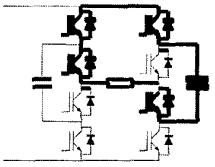
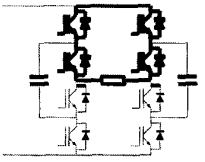
S_L \ S_R	00	01	10	11
00	 $V_{load} = 0V$	 $V_{load} = -V_{dc}/2$ C_{right} discharging	 $V_{load} = -V_{dc}/2$ C_{right} charging	 $V_{load} = -V_{dc}$
01	 $V_{load} = +V_{dc}/2$ C_{left} discharging	 $V_{load} = 0V$ C_{left} / C_{right} equalizing	 $V_{load} = 0V$ C_{left} / C_{right} equalizing	 $V_{load} = -V_{dc}/2$ C_{left} charging
10	 V_l $V_{oad} = +V_{dc}/2$ C_{left} charging	 $V_{load} = 0V$ C_{left} / C_{right} equalising	 $V_{load} = 0V$ C_{left} / C_{right} equalizing	 $V_{load} = -V_{dc}/2$ C_{left} discharging
11	 $V_{load} = +V_{dc}$	 $V_{load} = +V_{dc}/2$ C_{right} charging	 $V_{load} = +V_{dc}/2$ C_{right} discharging	 $V_{load} = 0V$

Figure 2: Switching States for a Three-Level Flying-Capacitor Inverter